MAGIC-TDAS 12-01
120102/JLLemus

The MAGIC Timing System (1st Version)

José Luis Lemus
<jllemus@gae.ucm.es>
Luis Ángel Tejedor
<luistejedor@gae.ucm.es>
Juan Abel Barrio
<barrio@gae.ucm.es>

Jan 2, 2012

Abstract

This document contains technical data about the new Timing System now installed in MAGIC. The system is, basically, an upgrade of that installed before in La Palma, whose mission was to timestamp the events recorded in both the telescopes. Among its characteristics are the same stability (it is based on a GPS disciplined Rubidium clock), more precision, simpler connectivity and a more compact design.

Contents

1 The old timing system

The old timing system consisted of several separate units, that is, the Rubidium clock (Rubclock), the GPS module and several NIM modules. The Rubclock provided, via the digital clock CADM, a 20-bit BCD time signal in *hhmmss* format (see table 1). From now on the *supersecond* signal.

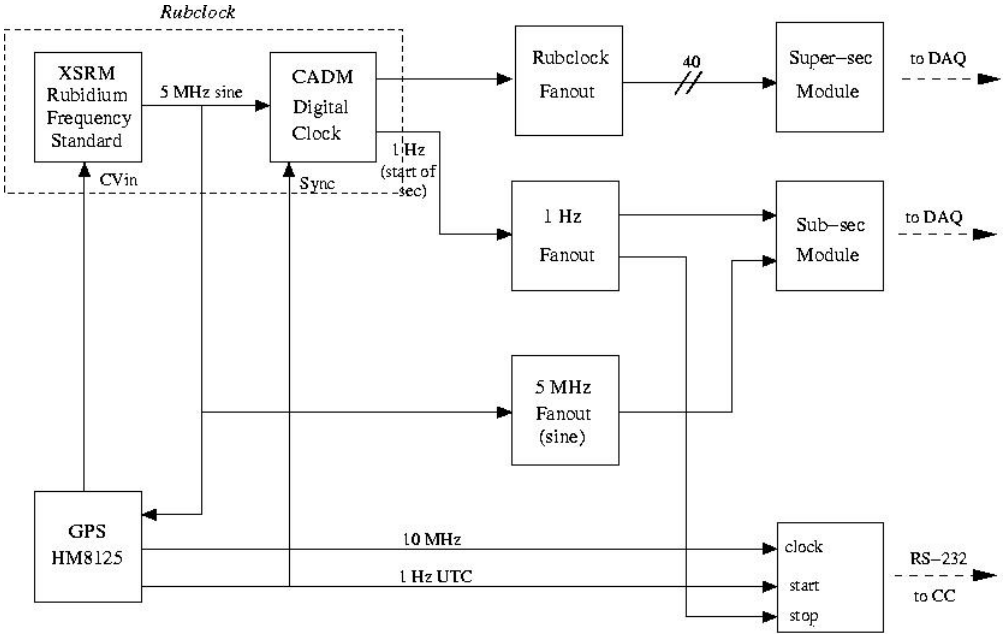


Figure 1: *Old Timing system diagram.*

In order to get a more precise *subsecond* timing, the Rubclock exported a high precision 5 MHz sinewave which was fed to a separate NIM module. This module converted the sine wave to TTL levels and counted the ticks with a 200 ns precision. Despite the Rubidium atomic clock, a minimum course error is unavoidable in a long time, so a GPS system was used to disciplinate the rubidium clock each second. The CADM provided a 1PPS signal that was used to reset the subsecond system at the beginning of every second.

To measure the difference in time between the CADM and the GPS, another NIM module was used that sent that difference codified over an RS-232 communication. That delay set the overall current Timing precision down to 1.5 μs.

The sub-second system provided a binary 24 bit signal meaning the number of 200 ns intervals counted until read. And the supersecond provided a 20 bit BCD signal as seen in table 1.

Bit	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	Hour decades		Hour units				Minute decades			Minute units				Second decades			Second units			

Table 1: *Supersecond bit distribution.*

Both the supersecond and subsecond signals are converted to LVDS format and fed to the Digital Modules in order to timestamp events, so the 44 bit LVDS signal (20 bits for supersecond and 24 for subsecond) required 88 physical cables divided into four connectors (three 40 pin connector and one 16

pin connector). Please, notice the LVDS polarity is wrong in some of the documentation, the correct pin distribution can be seen in table 2 of this document.

Subsecond				Supersecond			
Connector 1		Connector 2		Connector 1		Connector 2	
Pin pair	Signal	Pin pair	Signal	Pin pair	Signal	Pin pair	Signal
39-40	-	39-40	-	15-16	-	39-40	-
37-38	-	37-38	-	13-14	-	37-38	-
35-36	-	35-36	Bit 9	11-12	h dec. MSB	35-36	h unit
33-34	-	33-34	Bit 10	09-10	h dec. LSB	33-34	h unit LSB
31-32	-	31-32	Bit 11	07-08	h unit MSB	31-32	m dec. MSB
29-30	-	29-30	Bit 12	05-06	h unit	29-30	m dec.
27-28	-	27-28	Bit 13	03-04	-	27-28	m dec. LSB
25-26	-	25-26	Bit 14	01-02	-	25-26	m unit MSB
23-24	-	23-24	Bit 15			23-24	m unit
21-22	-	21-22	Bit 16			21-22	m unit
19-20	Bit 1 (LSB)	19-20	Bit 17			19-20	m unit LSB
17-18	Bit 2	17-18	Bit 18			17-18	s dec. MSB
15-16	Bit 3	15-16	Bit 19			15-16	s dec.
13-14	Bit 4	13-14	Bit 20			13-14	s dec. LSB
11-12	Bit 5	11-12	Bit 21			11-12	s unit MSB
09-10	Bit 6	09-10	Bit 22			09-10	s unit
07-08	Bit 7	07-08	Bit 23			07-08	s unit
05-06	Bit 8	05-06	Bit 24 (MSB)			05-06	s unit LSB
03-04	-	03-04	-			03-04	-
01-02	-	01-02	-			01-02	-

Odd pins for NEGATIVE LVDS level

Table 2: *Subsecond and Supersecond connectors pin distribution.*

2 The current timing system

The main idea was to substitute the Rubclock and GPS modules with a single timing solution that integrates both a Rubidium clock and a GPS timing system. Also, a new single Timing rack module contains both the subsecond and supersecond electronics for both telescopes, providing a cleaner disposition and easier operation.

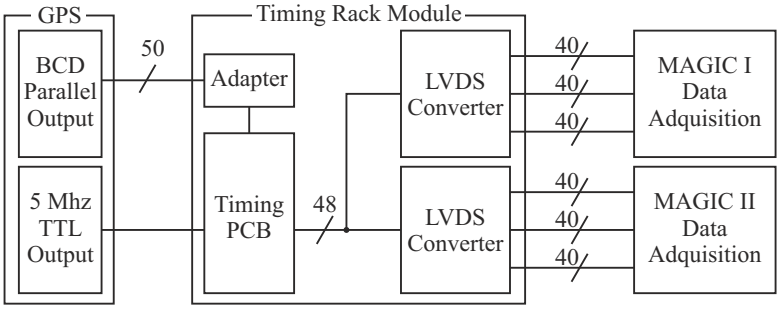


Figure 2: *New Timing block diagram.*

3 The GPS unit

The chosen model was the Symmetricom XLi[1], a GPS timing integrated system that provides all the goods of the former system and some more in a much more reduced space.

Figure 3: *Symmetricom^{TM}XLi rack unit.*

This rack unit provides:

- A highly precise internal Rubidium clock, used by the whole system as a master tick giver that provides a stability of 3×10^{-11} @ 1 second.
- A UTC corrected 1Hz TTL signal (better than 30 ns RMS accuracy to UTC according to manufacturers datasheet).
- Option Card 87-8034-1. Four configurable independent TTL outputs (1 PPS, 1 kPPS, 10 kPPS, 100 kPPS, 1 MPPS, 5 MPPS,10 MPPS).
- Option Card 86-8008. Four configurable independent TTL/sine outputs (1 MPPS/MHz, 5 MPPS/MHz, 10 MPPS/MHz).
- One 1 PPS, 10 PPS, 100 PPS, 1 kPPS, 10 kPPS, 100 kPPS, 1 MPPS, 5 MPPS, 10 MPPS TTL programmable output.
- A BCD *hhmmss* signal output with time quality for the super-sec.
- An independent NTP server with standard ethernet connection which would make the whole system more robust against internet failures.
- Intuitive web management, so the unit can be remotely controlled and monitored.

3.1 GPS front panel

The front panel of the GPS can be seen in figure 4. From left to right, it provides:

- A status LED. Its color is green if there is no problem and red if there is any alarm.
- A display showing the status of the GPS, the current time or the menu navigation.
- A keypad from which all of the functions of the GPS can be accessed. Please, read the GPS manual for more information.

[1] http://www.symmetricom.com/products/gps-solutions/gps-time-frequency-receivers/XLi/

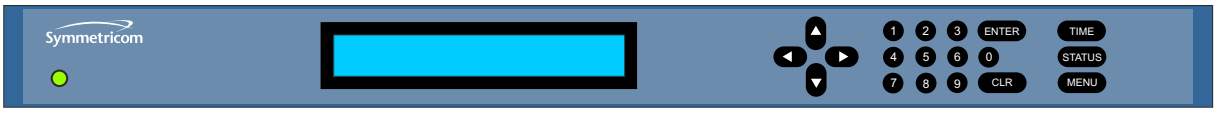


Figure 4: *GPS module front panel.*

3.2 GPS back panel

The back panel of the GPS can be seen in figure 5. From left to right you can see:

- The power socket.
- 4 configurable outputs (Option Card 87-8034-1).

  J1 Configured to: 10 kPPS

  J2 Configured to: 5 MPPS

  J3 Configured to: 1 PPS

  J4 Configured to: 10 MPPS

- 4 configurable outputs (Option Card 86-8008).

  J1 Configured to: 1 MHz kPPS

  J2 Configured to: 5 MPPS

  J3 Configured to: 1 MPPS

  J4 Configured to: 1 MHz

- The BCD output (which is connected to the Timing Module described in next section).
- The Antenna connector (which is connected to the Timing Module discussed in next section).
- The serial Input/output socket. Currently unused because we use the ethernet under it.
- J1 and J3 inputs, currently unused
- J2 programmable output. Configured to 5 MPPS to drive the subsecond counter.
- CODE and ALARM inputs, still unused.
- 1PPS signal output, currently used for the Central Pixel synchronization.

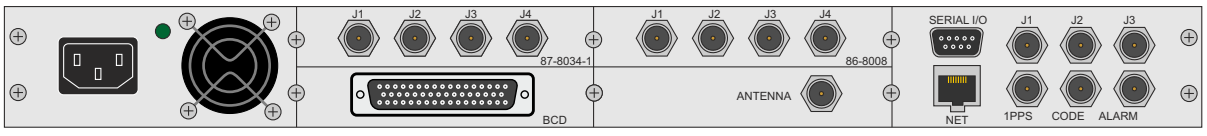


Figure 5: *GPS module back panel.*

3.3 Remote Operation

3.3.1 Network configuration

The GPS can be operated remotely via ethernet protocols. Its network configuration is:

IP: 161.72.130.67.

Broadcast: 161.72.130.127.

Mask: 255.255.255.128.

From within the internal network, the GPS can be also accessed with its domain name `timing.magic.iac.es`.

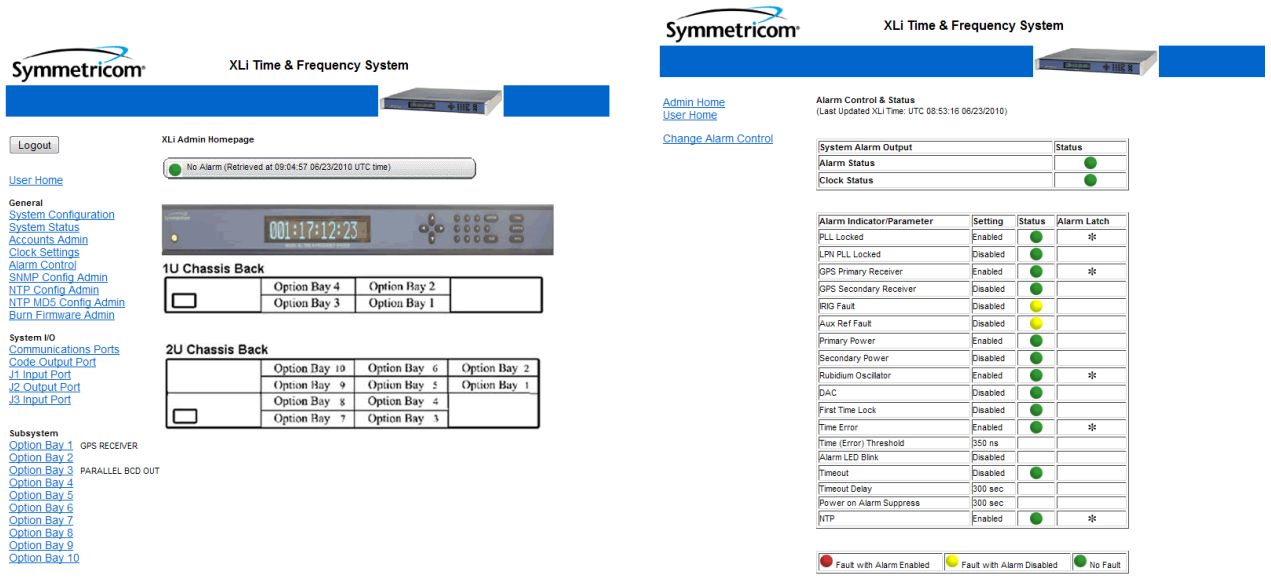
3.3.2 GPS web interface

Entering the Web Interface can be done by typing `http://161.72.130.67/` in a web Browser. There are two access modes: as Administrator and as User. In order to enter the system as an administrator the login and password are:

Login: MAGIC

Password: the standard MAGIC password

The GPS system can only be partially controlled via web. The look of the home of the web interface can be seen in figure 6 (a). In order to change any configuration accessible from the web, there is a menu to the left of the home page. The most common function is checking the alarm status, which can be accessed from the home page by clicking 'Alarm Control' and then 'Alarm Control/Status' (see figure 6 b).



(a) (b)

Figure 6: *Symmetricom^{TM}XLi web interface Home (a) and Alarm page (b).*

4 The Timing Rack Module

The Timing Rack Module contains all the electronics needed to export valid timing information in LVDS format for both MAGIC I and II. The previous idea of placing the subsecond and supersecond electronics in different modules has some advantages, but with the new GPS system there is no need to separate them and use that space consuming philosophy.

4.1 Timing Module's front panel

The module's front panel consist of several elements:

- Two sets of three connectors placed on the frontplate for each telescope.
- A power supply LED indicator and protection fuse for each PCB.
- An "Alarm" LED indicator and an "Alarm reset" button.

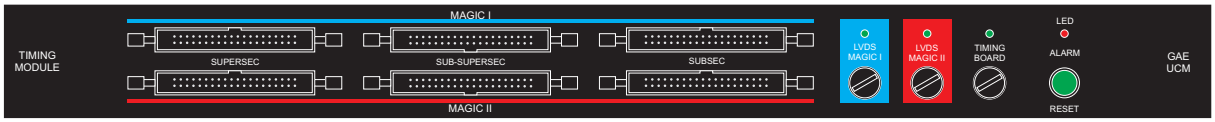


Figure 7: *Timing rack module front panel.*

The six 40 pin connectors (three for each telescope) provide the complete timestamp in LVDS format. Table 3 shows the pin distribution for each set. That way, the cable disposition is cleaner than the previous solution and the three LVDS ribbons can be brided together for an easier operation.

Supersec connector		
Pin pair	Description	Signal
01-02	–	GND
03-04	–	GND
05-06	Supersec 0	Seconds 0
07-08	Supersec 1	Seconds 1
09-10	Supersec 2	Seconds 2
11-12	Supersec 3	Seconds 3
13-14	Supersec 4	Tens-sec 0
15-16	Supersec 5	Tens-sec 1
17-18	Supersec 6	Tens-sec 2
19-20	Supersec 7	Minutes 0
21-22	Supersec 8	Minutes 1
23-24	Supersec 9	Minutes 2
25-26	Supersec 10	Minutes 3
27-28	Supersec 11	Tens-min 0
29-30	Supersec 12	Tens-min 1
31-32	Supersec 13	Tens-min 2
33-34	Supersec 14	Hours 0
35-36	Supersec 15	Hours 1
37-38	–	GND
39-40	–	GND
Odd pins for NEGATIVE LVDS levels		

Sub-supersec connector		
Pin pair	Description	Signal
01-02	–	GND
03-04	–	GND
05-06	Supersec 16	Hours 2
07-08	Supersec 17	Hours 3
09-10	Supersec 18	Tens-ho 0
11-12	Supersec 19	Tens-ho 1
13-14	–	0
15-16	–	0
17-18	–	0
19-20	–	0
21-22	Subsec 7	25600
23-24	Subsec 6	12800
25-26	Subsec 5	6400
27-28	Subsec 4	3200
29-30	Subsec 3	1600
31-32	Subsec 2	800
33-34	Subsec 1	400
35-36	Subsec 0	200
37-38	–	GND
39-40	–	GND
Odd pins for POSITIVE LVDS levels		

Subsec connector		
Pin pair	Description	Signal
01-02	–	GND
03-04	–	GND
05-06	Subsec 8	51200
07-08	Subsec 9	102400
09-10	Subsec 10	204800
11-12	Subsec 11	409600
13-14	Subsec 12	819200
15-16	Subsec 13	1638400
17-18	Subsec 14	3276800
19-20	Subsec 15	6553600
21-22	Subsec 16	13107200
23-24	Subsec 17	26214400
25-26	Subsec 18	52428800
27-28	Subsec 19	104857600
29-30	Subsec 20	209715200
31-32	Subsec 21	419430400
33-34	Subsec 22	838860800
35-36	Alarm	Alarm Flag
37-38	–	GND
39-40	–	GND
Odd pins for NEGATIVE LVDS levels		

Table 3: *LVDS Connectors pin distribution.*

The connector standard used is compatible with IDC, for a clearer view of the pin disposition in the actual connector, see figure 8.

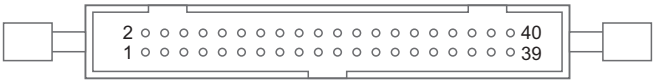


Figure 8: *40 pin latched IDC connector for LVDS outputs (front view).*

To the right of the LVDS connectors, there are three sets consisting of a LED and a fuse, corresponding to each of the PCBs inside the module. Each of these three green LEDs are on if there is not any problem with the power supply of that particular board. When the LED is off, the first thing to do is check if the fuse needs to be replaced. There is a Troubleshooting section to know what must be done in any case. All three fuses are cylindrical 5x20 mm and their current limit is 500 mA.

4.2 Timing Module's back panel

The back panel of the Timing Rack Module consists of:

- The power supply input and ON/OFF switch.
- The GPS TTL BCD timing input.
- A 5 MHz TTL clock input.

Figure 9: *Timing rack module back panel.*

4.3 Timing Module's inner distribution

The Timing Rack Module contains several electronic boards:

- The Timing Board.
- The Alarm board.
- Two LVDS converter boards.
- The power supply board.
- The Adapter board.

4.3.1 The Timing Board

Regarding the electrical operation it performs, the Timing board can be divided in two sections, the Supersecond section and the Subsecond section.

The Supersecond section obtains its data from the GPS BCD parallel output module and uses the 1 PPS Strobe signal to latch the data (see subsection 5.2) and then route them to the output standard

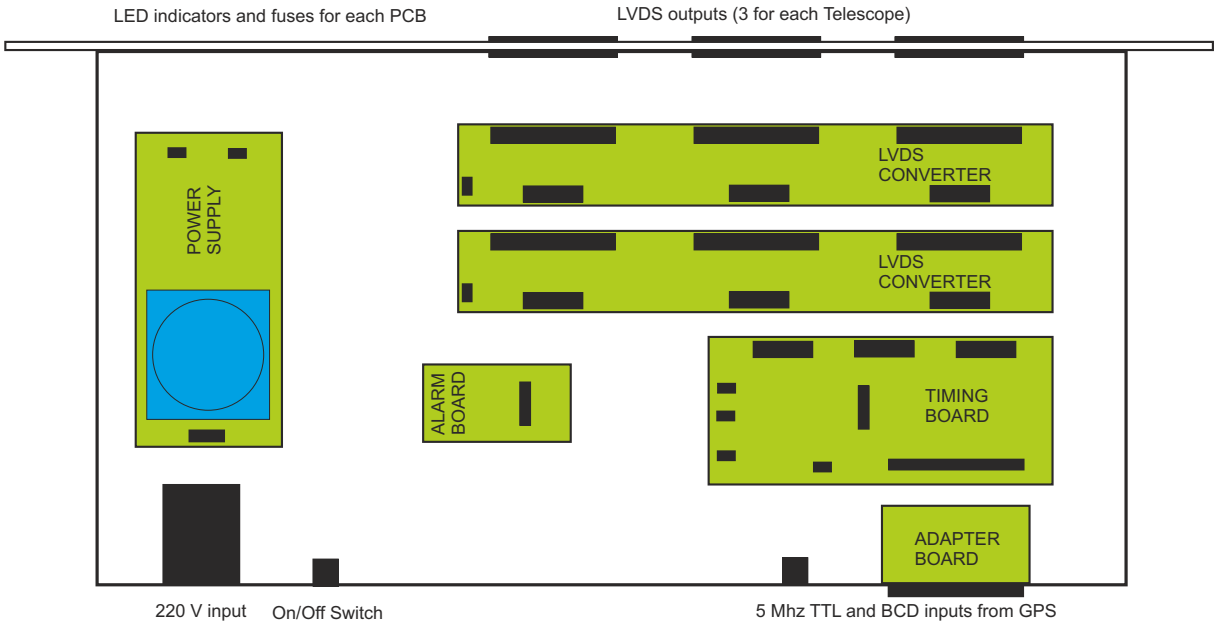


Figure 10: *Timing rack module inner distribution.*

Pin	Output	Pin	Output
1	Ground	26	Minute Decades LSB
2	-	27	Minute Units MSB
3	Day Hundreds MSB	28	Minute Units
4	Day Hundreds LSB	29	Minute Units
5	Day Decades MSB	30	Minute Units LSB
6	Day Decades	31	Second Decades MSB
7	Day Decades	32	Second Decades
8	Day Decades LSB	33	Second Decades LSB
9	1KPPS Strobe	34	Second Units MSB
10	Day Units MSB	35	Second Units
11	Day Units	36	Second Units
12	Day Units	37	Second Units LSB
13	Day Units LSB	38	Millisecond Hundreds MSB
14	Time Quality Bit 2	39	Millisecond Hundreds
15	Time Quality Bit 3	40	Millisecond Hundreds
16	1PPS Strobe	41	Millisecond Hundreds LSB
17	Time Quality Bit 4	42	Millisecond Decades MSB
18	Hour Decades MSB	43	Millisecond Decades
19	Hour Decades LSB	44	Millisecond Decades
20	Hour Units MSB	45	Millisecond Decades LSB
21	Hour Units	46	Millisecond Units MSB
22	Hour Units	47	Millisecond Units
23	Hour Units LSB	48	Millisecond Units
24	Minute Decades MSB	49	Millisecond Units LSB
25	Minute Decades	50	Time Quality Bit 1

Table 4: *GPS BCD parallel output pins.*

IDC connectors used inside the module. The GPS BCD module provides a 50-pin signal (see table 4) of which the Timing board uses 22. Divided as follows: 20 bits for *hhmmss* coding (pins 18 to 37), a GND signal (pin1) and the 1PPS strobe 'data valid' signal (pin 16).

The Subsecond system is based on the previous design –which was based on the HEGRA 5 MHz TIC– of the MAGIC timing system and consists of three 8 bit counters that use as a clock the 5 MHz TTL output of the GPS-Rubidium clock system and are reset every second by the 1PPS strobe.

In the former sub-second system there were 24 bits (over 16 million codes) dedicated to the sub-second counter, nevertheless there can be only 5 million intervals of 200 ns in a second, so one of the bits is unnecessary. With the first 23 bits (over 8 million codes) is more than enough to code the *sub-second* information and the spare bit is used for an 'alarm' flag.

4.3.2 The Alarm Board

The alarm system works as follows: If there was a problem with any of the inputs of the module –a loosen wire, an incredibly powerful interference– then the counters could go over one second count before being reset, therefore invalidating any timing data acquired in that period. With a simple combinational logic, the alarm circuit detects an over–one–second count and puts a '1' in the 24^{th} bit of every package received in that period. Furthermore, as that would indicate an error in the global timestamp, the red alarm LED on the Timing module will turn on and keep in that state until the next 1PPS signal resets it. If the system is not receiving the 1PPS signal, the alarm LED will keep on until 'reset alarm' button is pressed and all the timestamp data will be flagged as unreliable.

4.3.3 The LVDS converter Boards

All the Timestamp data is converted to LVDS format by a LVDS Converter Board. There are two boards inside the unit, one for each telescope, that can convert up to 48 TTL signals to LVDS. Each board has three 16 pin TTL inputs and three 40 pin LVDS outputs (see table 5) in which the odd pins are used for the positive LVDS level.

LVDS Converter	
LVDS outputs	TTL Inputs
39-40	–
37-38	–
35-36	TTL input 16
33-34	TTL input 15
31-32	TTL input 14
29-30	TTL input 13
27-28	TTL input 12
25-26	TTL input 11
23-24	TTL input 10
21-22	TTL input 9
19-20	TTL input 8
17-18	TTL input 7
15-16	TTL input 6
13-14	TTL input 5
11-12	TTL input 4
09-10	TTL input 3
07-08	TTL input 2
05-06	TTL input 1
03-04	–
01-02	–

Odd pins for positive LVDS level

Table 5: *LVDS Converters pin distribution.*

4.3.4 The Power Supply Board

The Power Supply Board is a dual linear supply with two outputs:

- 5 V dc @ 1.5 A for the Timing and Alarm boards
- 3.3 V dc @ 1.5 A for the LVDS converter boards

The AC power is driven through an EMI filter into a toroidal transformer in order to minimize the noise. The output of the tranformer is then rectified by ultra-fast diodes and stabilized by a linear regulator. The result is a clean power supply that can easily cope with the needs of the Timing Module.

5 The GPS – Module interaction

5.1 Delay compensation

Although the GPS provides a 1PPS accurate to UTC signal, the BCD parallel output is not inmediate, in fact the BCD signal does not change synchronously with the 1PPS UTC signal but some $t_{\text{processing}}$ later (the manufacturer's datasheet indicates $\leq$100 ns). If this signal was used to reset the subsecond counter, there would be a small time interval in which subsecond and supersecond system may not provide a valid timestamp (see figure 11-a).

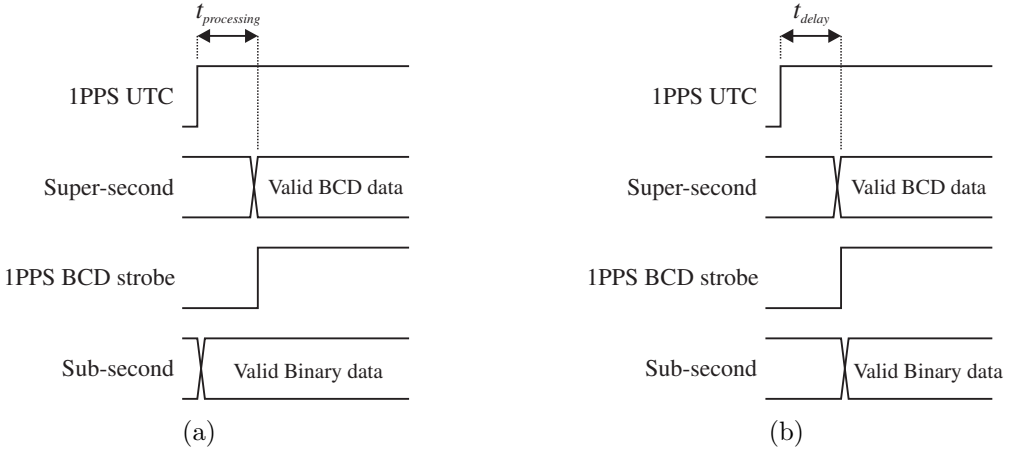


Figure 11: *Time diagram using the 1PPS UTC (a) and the 1PPS BCD strobe signal (b) to reset the subsecond counter*

In order to solve this issue, the subsecond system needs to be delayed to concur with the supersecond. The BCD parallel system provides a 1PPS strobe pin which indicates that there is a valid BCD time signal at the output pins. This strobe is used to reset the counters in the subsecond system, so they start counting *after* the supersecond has stabilized. This way timestamps are valid, but delayed.

It may seem one problem is solved by causing another one, but in fact the latter has definitive solution, which is measuring the time interval between the 1PPS UTC and the 1PPS BCD signals and increasing the final timestamp by that number. In the former system, this number could be as high as 1.5 μs, but with the new GPS that number is negligible compared to the overall system resolution (measured time is around 65 ns, see figure 12), so monitoring this t_{delay} should be unnecessary.

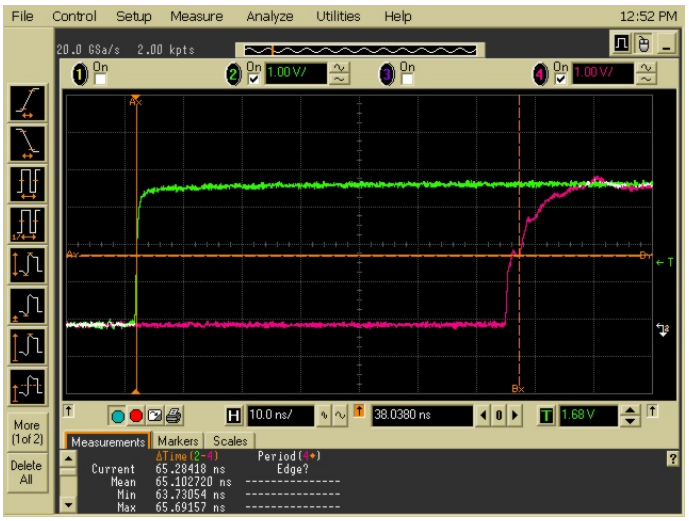


Figure 12: *Time difference between 1PPS strobe (magenta) and 1PPS UTC (green) signals*

5.2 Supersecond latching

After installing the new Timing system, we found that there was a problem with the Supersecond signal exported by the GPS. In order to put a valid BCD signal at the output in time, we discovered that the bits start changing *before* the 1 PPS signal arrives, instead of changing all simultaneously. That behaviour caused a glitch in the system, in which there was a period of time (namely 50 ms) where the Supersecond signal had already changed before the Subsecond did. This could be seen in some of the graphs captured from the MAGIC 1 DAQ (see figure 13).

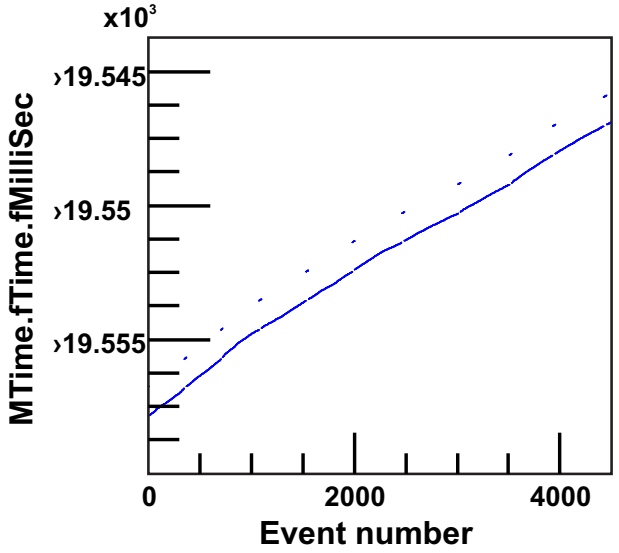


Figure 13: *Time glitch in the new Timing system*

The solution was to force all the bits in the Supersecond output to change simultaneusly. We used a hi-speed latch to do so using the 1 PPS strobe as the Latch Enable signal (see figure 14).

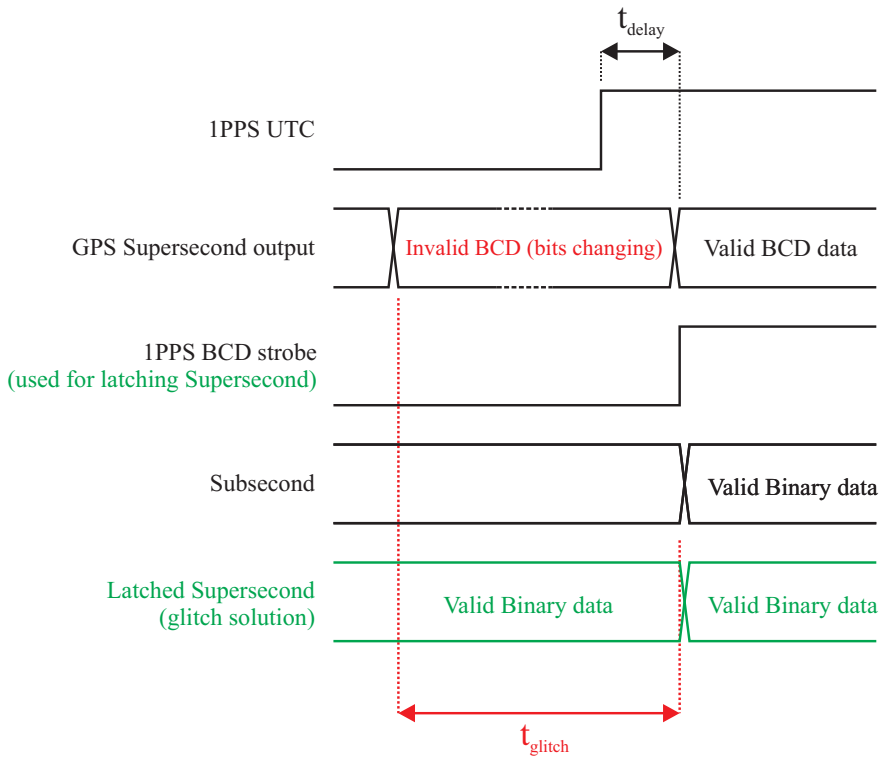


Figure 14: *Glitch time diagram and solution*

5.3 Supersecond overvoltage

After installing the Supersecond Latching system, we found that there was another problem with the counters. They stopped counting instead of being reset. A few measurements were done at La Palma, where we found that the GPS was delivering 6V signals instead of 3.3V signals. It was fixed on site but after contacting Symmetricom, they did some tests in their labs and confirmed that the BCD module was delivering the wrong voltage. Although they offered a couple of solutions, the fastest workaround was to lower the voltage of each of the BCD signals with a simple voltage divider with a low pass filter to avoid peaks.

6 Troubleshooting

In this section are listed some of the proceedings in case of malfunction of the Timing Module. The first step to take is to replace the Timing Module with its spare. In case the spare is not available, follow the troubleshooting flowchart.

6.1 General Troubleshooting flowchart

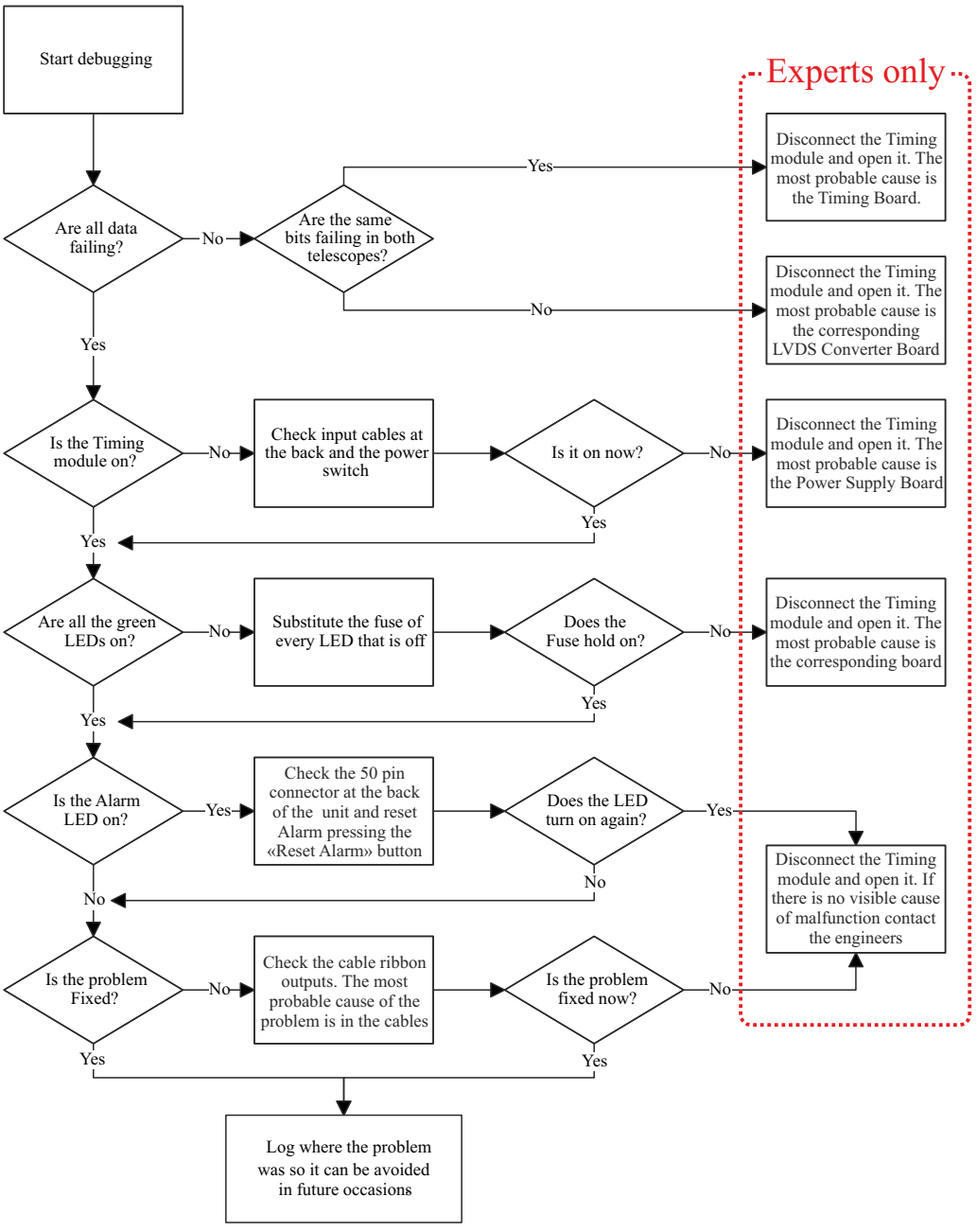


Figure 15: *General Troubleshooting flow chart.*

A Timing Module schematics and PCB layouts

A.1 Timing Board

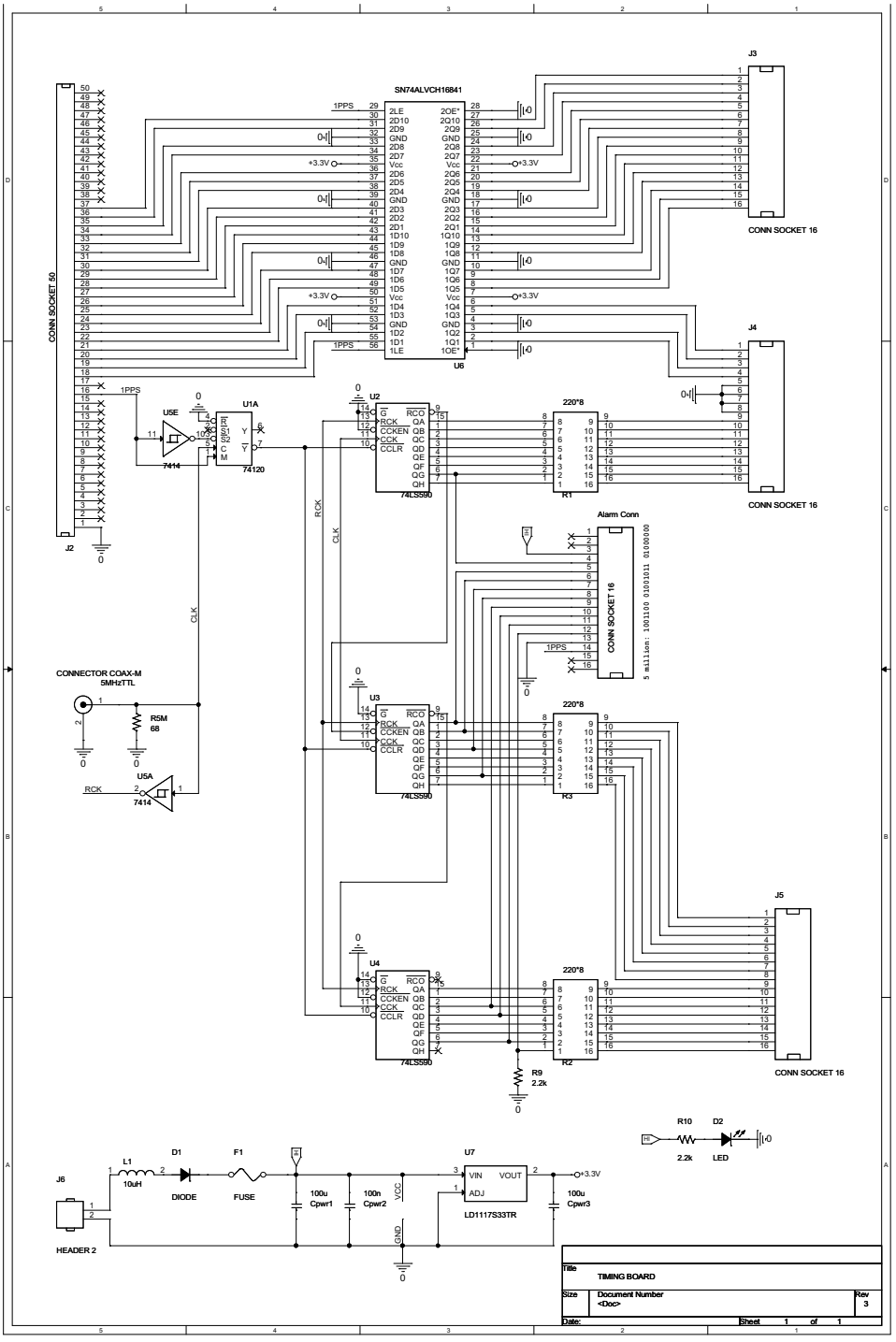


Figure 16: *Timing Board schematic.*

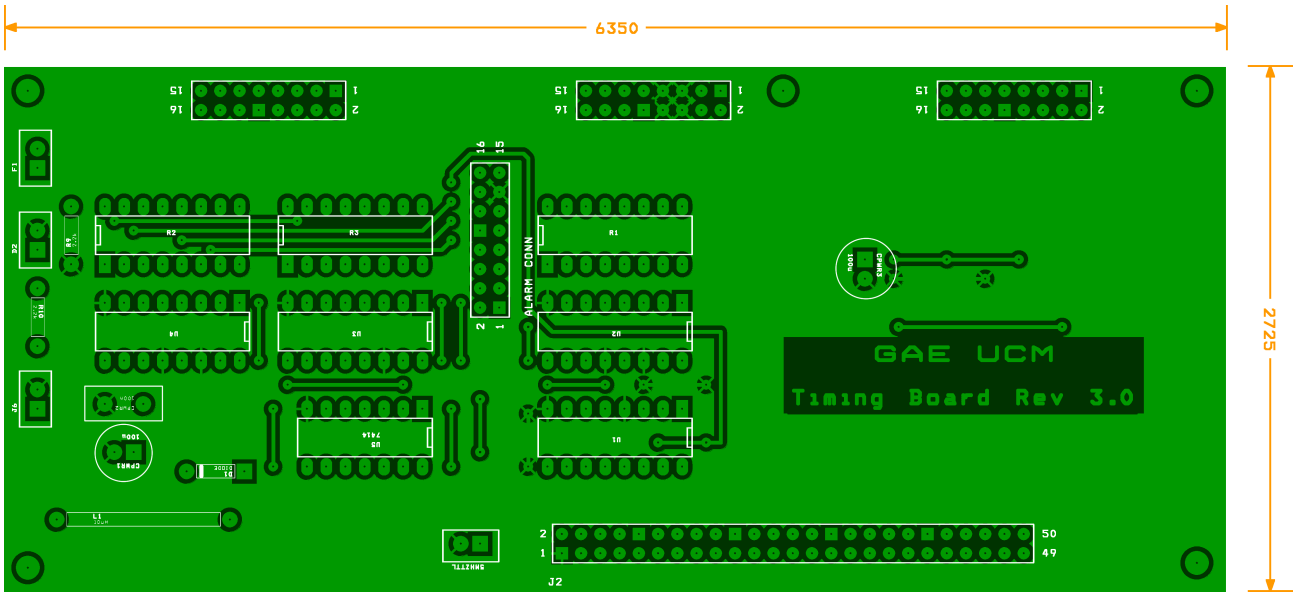


Figure 17: *Timing Board PCB layout (Top side).*

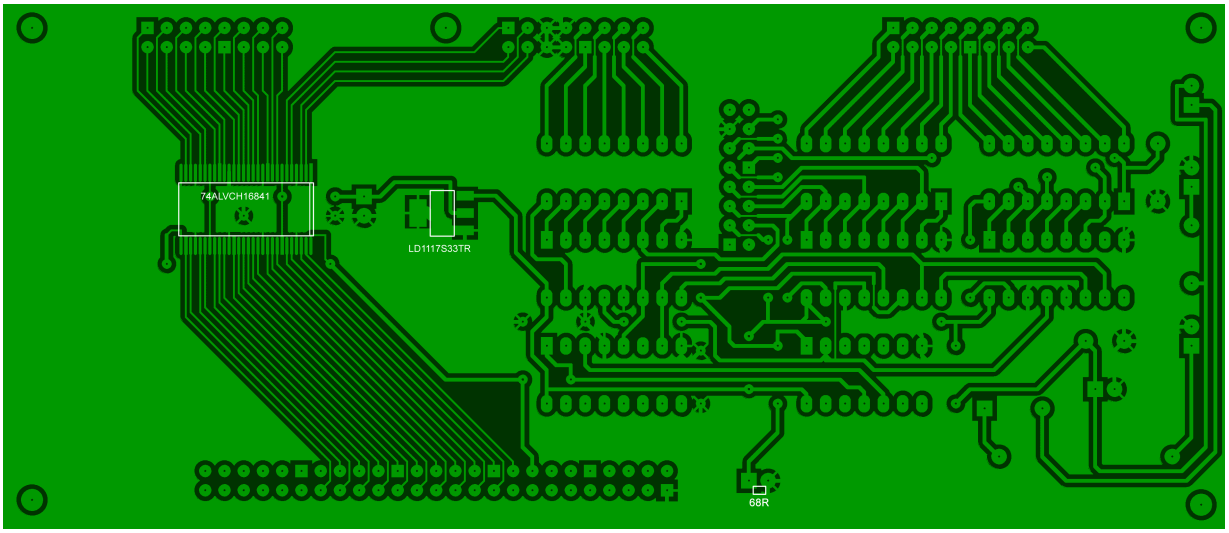


Figure 18: *Timing Board PCB layout (Bottom side).*

A.2 Alarm Board

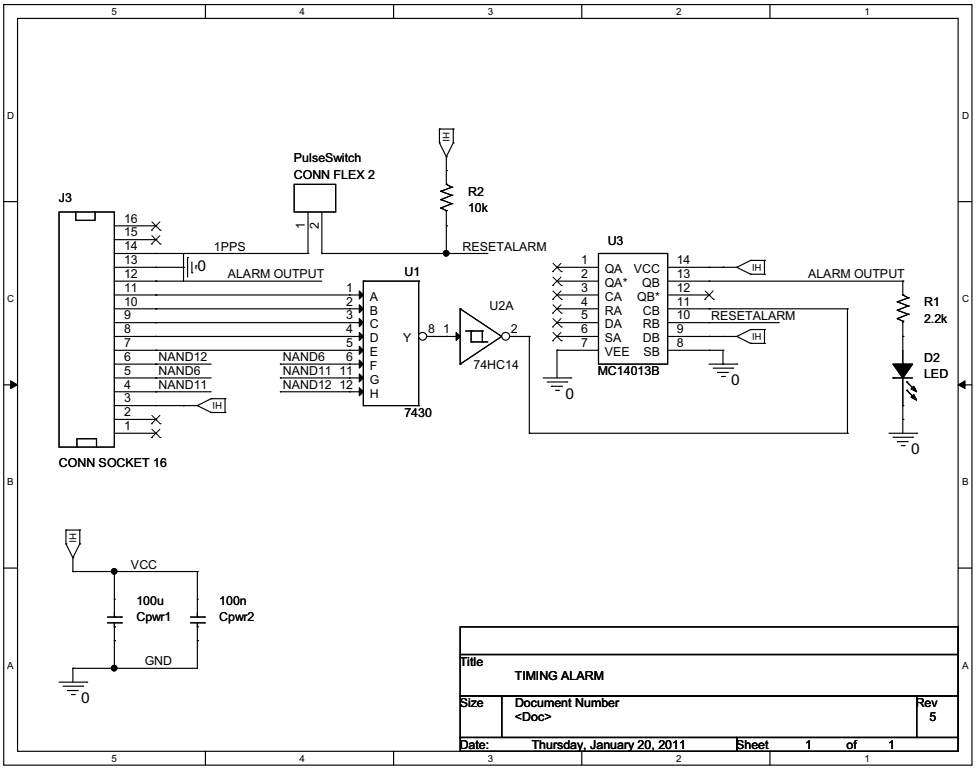


Figure 19: *Alarm Board schematic.*

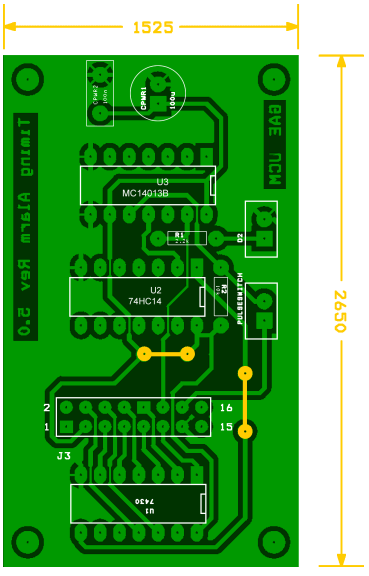
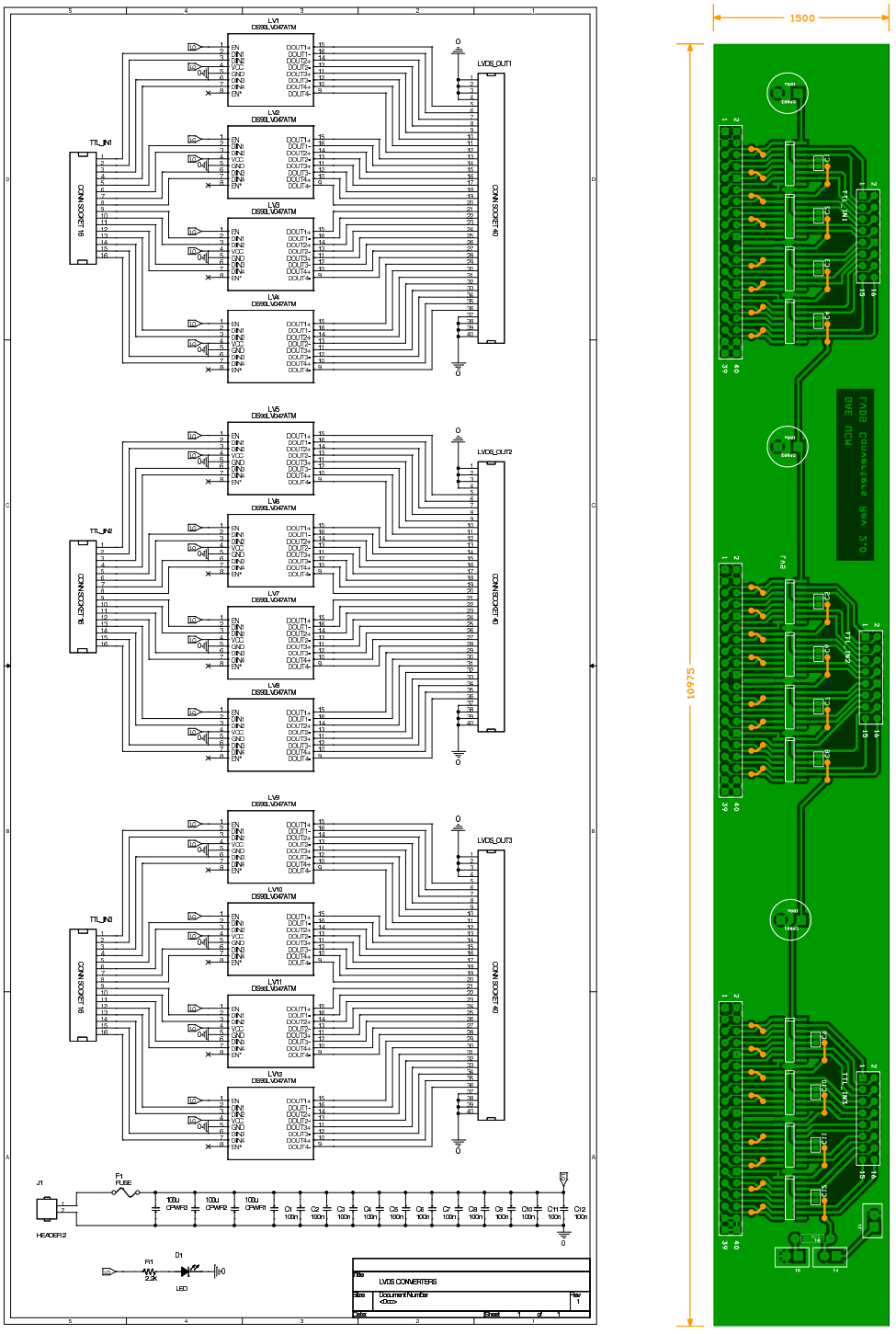


Figure 20: *Alarm PCB layout.*

A.3 LVDS Converters Board



(a) (b)

Figure 21: *LVDS Converters Board schematic (a) and PCB layout (b)*

A.4 Power Supply Board

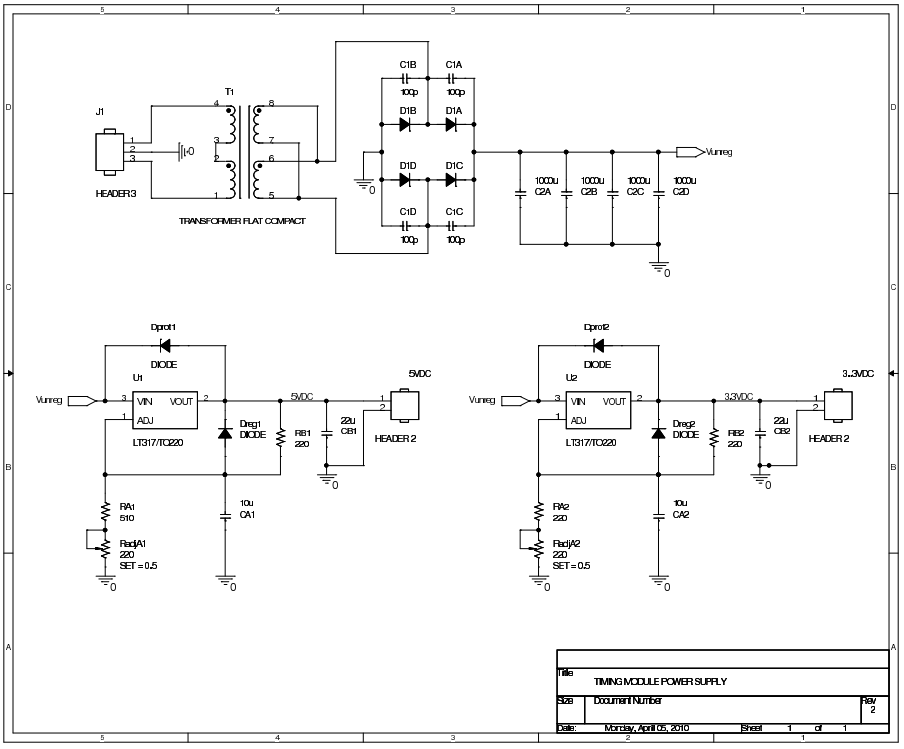


Figure 22: *Power Supply Board schematic.*

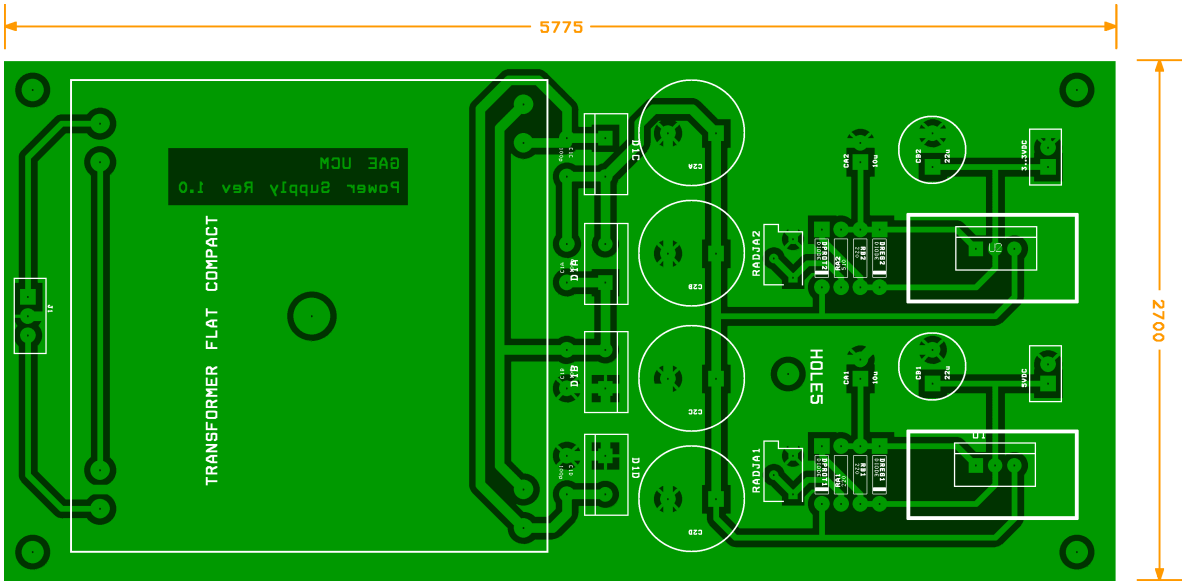


Figure 23: *Power Supply Board PCB layout.*

B GPS network configuration and communication program

B.1 GPS alarm script

Here is a listing of the code of the script that checks the alarm of the GPS via Telnet (ask GAE-UCM for password <gae-hardware@gae.ucm.es>):

```
#!/usr/bin/expect -f
#/usr/bin/expect is the directory where expect was installed
######################################################################
#
#  Timing Alarm Status checker, via telnet
#
######################################################################

log_user 0
####this command is used to hide the conversation

# set address timing.magic.iac.es
set address 161.72.130.67
set username operator
set password ### Ask GAE-UCM for password <gae-hardware@gae.ucm.es>


spawn telnet ${address}


###start conversation with the GPS:
expect "USER NAME:"
send -- "${username}\r"
expect "PASSWORD:"
send -- "${password}\r"
expect "LOGIN SUCCESSFUL!"
send -- "F73\r"
expect "F73\n"
expect "*"
set alarm_output $expect_out(0,string)
expect ">"
send -- "EXIT\r"
puts $alarm_output
###end the telnet session and exit the script
```