MAGIC
Major Atmospheric
Gamma Imaging
Cerenkov Telescopes

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LT1 BACKPLANE v.2.2 MEASUREMENTS

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1 Introduction

In physics environments, the trigger system is an essential part of any detector, because it rejects noise and fake events from the good ones. Often it has to manage a lot of channels, so a modular design is the only possible solution. That requires a backplane which accepts and afterwards distributes the signals coming from the sensors. In this report, a description of measurements and analysis, performed on the new LT1 (*Level Trigger 1*) [1] backplane (version 2.2) of the MAGIC Telescopes, is presented.

2 LT1 description

LT1 is a full digital system that works asynchronously, handling 559 digitalized short signals, generated by as many photomultipliers (PMTs). These PMTs cover the central region of the MAGIC camera [2] and are divided in 19 sub regions, called macrocells, partially overlapped (Fig.1). Each macrocell is an hexagon composed by 37 pixels (one blind) and data produced inside is processed by one single LT1-board[1].

The signal's length, at LT1 level, is very short, typically $\sim 5-6\,$ns, with a rise time of $\sim 1\,$ns. In average, the signal's frequency at the input is $\sim 1\,$MHz, while the trigger rate is $\sim 200\,$Hz. Therefore the rejection ratio is $\sim 10^4$. One of the most important parts of the system is the backplane, a huge PCB that hosts all the LT1-boards.

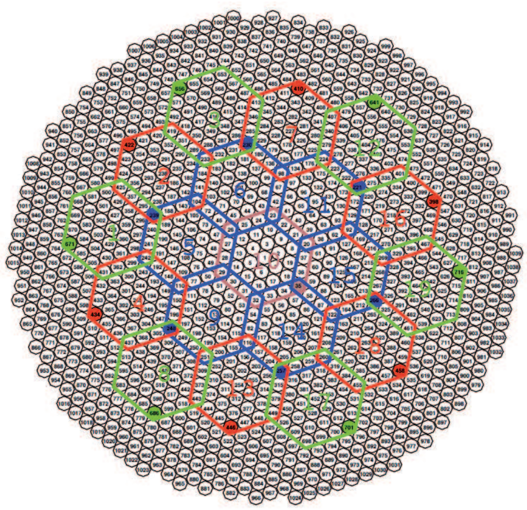

Figure 1: The trigger region composed by 559 PMTs, divided in 19 sub-regions.

3 Backplane

The Backplane is simply the motherboard (Fig.2) of the LT1, which distributes the PMTs pulse to the right LT1-board, for the final selection. The main aim is to send each signal to the proper macrocell, keeping the timing information and the signal integrity. Features as low skew, low crosstalk and high bandwidth are fundamental.

LVDS [4] is the signal format. It guarantees high common noise rejection, low power consumption, no reflections and high speed. The

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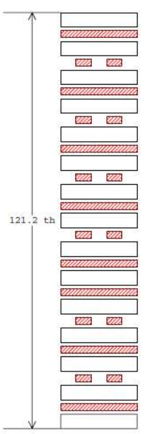
[1]The LT1-board is a PCB based on PLDs (*Programmable Logic Device*) [3], where the trigger selection's algorithm runs.

Figure 2: One LT1-board plugged in the Backplane.

input stage is formed by 70 connectors *MDR 10220-6212* and 204 LVDS buffers *FIN 1104*, while the output by 19 connectors 96 poles *DIN 41612*. The electricity supply is 3.3 V and the peak current consumption is less than $\sim$ 35 A. The PCB's dimensions are considerable: 430.53 mm x 425.70 mm x 3.078 mm (h x l x d). The stack-up (Fig.3) is made by 14 layers, whereof six are for signal routing. The trace's width is 4 mils, the differential line impedance is $\sim 100\,\Omega$ and the minimum distance between two lines is fixed to 2.5 times the trace's width.



NN	Layer Name	Type	Usage	Thickness th	Er
1	DIELECTRIC_1	Dielectric	Substrate	3	1
2	PLANE_1	Metal	Solid Plane	1.4	<Auto>
3	DIELECTRIC_3	Dielectric	Substrate	8	4.3
4	SIGNAL_2	Metal	Signal	0.7	<Auto>
5	DIELECTRIC_5	Dielectric	Substrate	8	4.3
6	PLANE_3	Metal	Solid Plane	0.7	<Auto>
7	DIELECTRIC_7	Dielectric	Substrate	8	4.3
8	SIGNAL_4	Metal	Signal	0.7	<Auto>
9	DIELECTRIC_9	Dielectric	Substrate	8	4.3
10	PLANE_5	Metal	Solid Plane	0.7	<Auto>
11	DIELECTRIC_11	Dielectric	Substrate	8	4.3
12	SIGNAL_6	Metal	Signal	0.7	<Auto>
13	DIELECTRIC_13	Dielectric	Substrate	8	4.3
14	PLANE_7	Metal	Solid Plane	0.7	<Auto>
15	DIELECTRIC_15	Dielectric	Substrate	8	4.3
16	SIGNAL_8	Metal	Signal	0.7	<Auto>
17	DIELECTRIC_17	Dielectric	Substrate	8	4.3
18	PLANE_9	Metal	Solid Plane	0.7	<Auto>
19	DIELECTRIC_19	Dielectric	Substrate	8	4.3
20	PLANE_10	Metal	Solid Plane	0.7	<Auto>
21	DIELECTRIC_21	Dielectric	Substrate	8	4.3
22	SIGNAL_11	Metal	Signal	0.7	<Auto>
23	DIELECTRIC_23	Dielectric	Substrate	8	4.3
24	PLANE_12	Metal	Solid Plane	0.7	<Auto>
25	DIELECTRIC_25	Dielectric	Substrate	8	4.4
26	SIGNAL_13	Metal	Signal	0.7	<Auto>
27	DIELECTRIC_27	Dielectric	Substrate	8	4.4
28	PLANE_14	Metal	Solid Plane	1.4	<Auto>
29	DIELECTRIC_29	Dielectric	Substrate	3	1

Figure 3: The stack-up scheme of Backplane v.2.2.

4 Measurements

In this section the following measurements are presented:

1. Characterization of the test equipment
2. Backplane jitter
3. Channels skew
4. Eye pattern diagram
5. Crosstalk

The test equipment used for these measurements is composed by a Digital Signal Generator *Tektronix DTG 5274* coupled with one differential output module *DTGM30*, an oscilloscope *DSO Agilent Infinium 54855* and a differential probe *Agilent 1134* (Fig.4).

Figure 4: On the left of the picture the Signal Generator and the oscilloscope, while on the right the LT1 system, lacking of LT1-boards.

4.1 Characterization of the test equipment

Some of the most important aspects of an instrument are the range of work and the stability. The Signal Generator plus the differential output can provide short pulses of less than 1 ns (maximum frequency 1, 35 GHz), with a slew rate higher then 2.25 V/ns. The oscilloscope has a bandwidth of 6 GHz and a real time sample rate per channel of 20 GSa/s, while the *Agilent 1134* is an active probe with a bandwidth of 7 GHz. Using an adapter board (Fig.5), made by two SMA connectors and the active probe, the instrumentation[2] jitter was measured. After three days of measurements, mainly concerning the channels skew, the temperature drift was very low. The timing test was repeated with a maximum variation of ~ 5 ps.

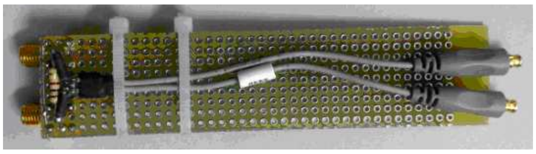


Figure 5: A picture of the adapter board used for the jitter measurements.

The generated signal[3] (Fig.6 & Fig.7) of 5 ns is read at the resistive termination, soldered between the two SMA connectors.

Figure 6: The signal provided by the Digital Signal Generator.

Activating the function *Jitter Histogram*, an estimation of the jitter (Fig.8) introduced by the test equipment, is done: 31 ± 4 ps.

[2]The instruments are connected in this way: Signal Generator ⇒ 2 x 1 m *RG184* cable w/SMA ⇒ adapter board ⇒ Agilent probe ⇒ Agilent oscilloscope.

[3]The loaded DTG settings file is "dazzi_data.dt".

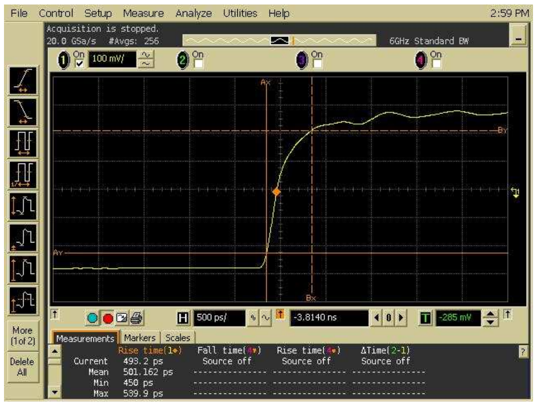


Figure 7: The rise time signal provided by the Digital Signal Generator.

Figure 8: Jitter contribution due to the test equipment.

4.2 Backplane jitter

In order to measure the total jitter[4], the adapter board was removed and the pulse generator was connected directly to the Backplane via a custom connector (Fig.9).

The Backplane output signal is acquired using a second hand-made board (Fig.10), where the probe's terminals are soldered on a resistive termination of $\sim 100\,\Omega$.

The Backplane output signal[5] (Fig.11) presents a jitter of 44 ± 5 ps (Fig.12), which is due to the contribution of the test equipment and Backplane. Considering that both two sources of jitter are independent and are

[4]The jitter due to the test equipment plus Backplane.

[5]M1_6 ⇒ Channel #6 in macrocell #1

Figure 9: An image of the connector used to adapt SMA to MDR format.

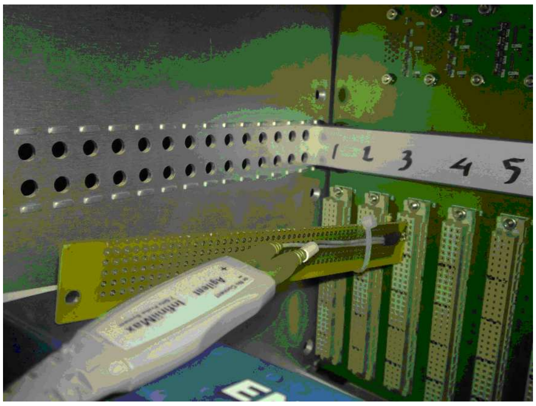


Figure 10: The image of the custom board, which hosts the differential probe.

a measure of tolerance, they add linearly. On end the Backplane's jitter is:

$$
\begin{aligned}
|Jit_{Backp.}| &= |Jit_{Tot.}| - |Jit_{Equip.}| \\
&= 44 - 31 \\
&= 13\,ps
\end{aligned}
$$

4.3 Channels skew

The relative timing difference is measured keeping, as a reference, the internal trigger of Digital Signal Generator. Periodically, the channel #1 in MDR connector J1 (output M1_6), was monitored to check the system's stability. The delays are calculated activating the average mode (256 samples) in the oscilloscope. In order to have the best scale resolution, the trigger was artificially delayed[6] and synchronized with the monitoring channel. The maximum skew recorded is 360 ps and the rms of skew distribution (Fig.13) is 67 ps.

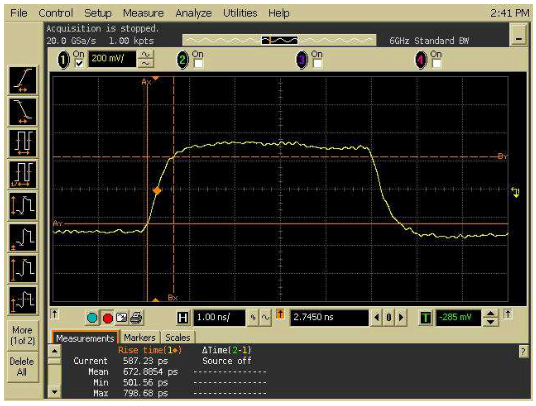


Figure 11: The output signal from macrocell #1 channel #6.

Figure 12: Jitter contribution due to the test equipment plus backplane.

The main causes of skew are:

- The different wires length. The constrain set during the routing is $\pm\,250$ mils, that corresponds to ~ 100 ps.
- The internal skew on the LVDS buffers. Data sheet reports a maximum value of 150 ps.
- Variation of input capacitance due to the

[6] Enabled function *skew* into channel menu of the oscilloscope.

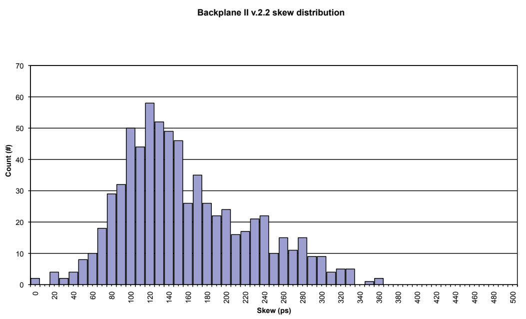


Figure 13: The channels skew distribution of Backplane v.2.2.

different splitting number. The input capacitance of LVDS buffer is 2.1 pF, which increases to 4.2 pF or 6.3 pF in case of triple split. In terms of picoseconds, it means about ~ 100 ps.

Most of the signals are not split and are connected to a single port of LVDS buffer, but someone is splitted two or even three times. That causes an enhancement of the capacitance load, slowing down the signal. In figure 14, it is simple to distinguish three different populations. Every time the capacitance increases, also skew increases. If only one population is considered, the timing spread is never more than $\sim$ 200 ps, which is in agreement with PCB and components specifications.

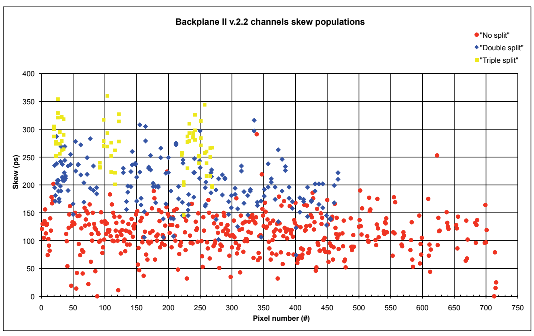


Figure 14: The skew distribution distinguished in three different populations, related to the splitting number.

4.4 Eye pattern

The pattern function PRBS7 (*Pseudo Random Binary Sequence of* 2^7*-1 length*) of Digital Signal Generator was used to test both maximum accepted rate and the jitter's influence on Backplane. This pattern generates a signal stream useful for the port receiver stress test and BER (*Bit Error Ratio*). It is injected on first channel of connector J1 and the output (M1_6) is read with the oscilloscope in "Eye Patter" mode. In figures 15, 16, 17 and 18, the behavior at different rates is shown.

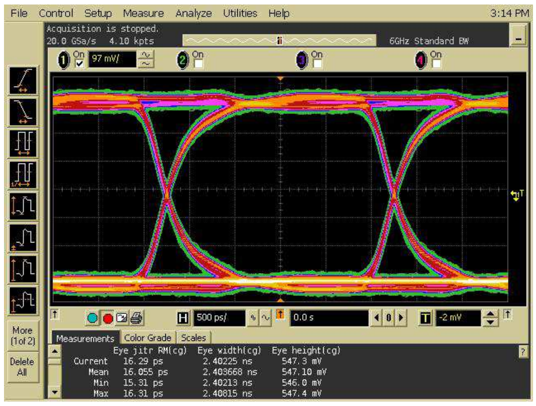


Figure 15: The eye pattern at 400 Mb/s.

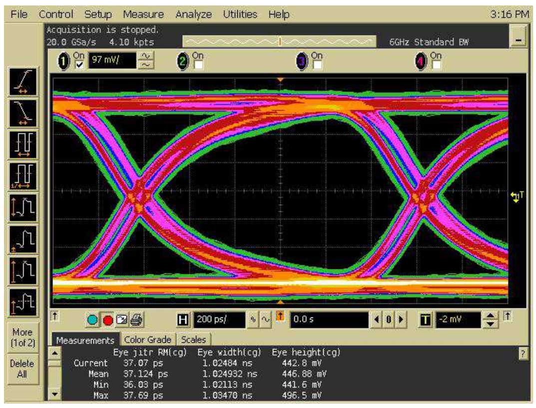


Figure 16: The eye pattern at 800 Mb/s.

There are not available eye diagrams beyond the rate of 1.05 Gb/s because the oscilloscope PLL stops and the clock recovey system doesn't recognize where the main data clock transition occurs. Another test to verify the maximum frequency, is performed stim-

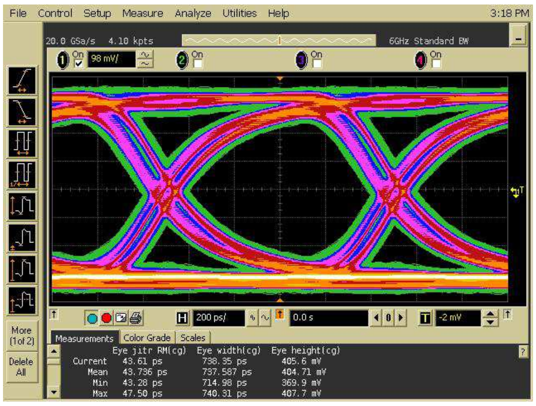


Figure 17: The eye pattern at 1 Gb/s.

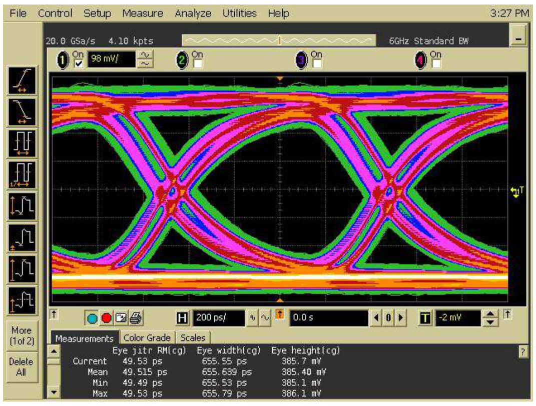


Figure 18: The eye pattern at 1.05 Gb/s.

ulating the Backplane with a pattern of six equal pulses (Fig.19), spaced out following a progressive scheme, from $1/5 \cdot \mathrm{Width}_{\mathrm{pulse}}$ to $1 \cdot \mathrm{Width}_{\mathrm{pulse}}$. The pulse's width is fixed to be 5 times the duration of the pulse generator clock. This simulates short and close events from PMTs.

With a clock rate of 1.2 Gb/s the system starts to loose events, because the signal slew rate is to low to reach the minimum LVDS level[7], before the following commutation. The figure 20 shows the stream of bits at the output, while figure 21 is a zoom of the previous image.

This result is excellent, because the Backplane supports a bit rate stream of 1 Gb/s

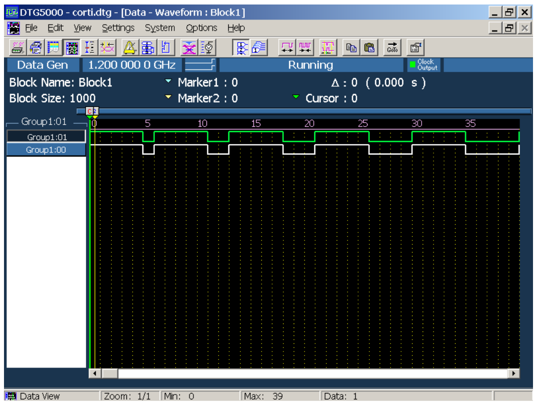


Figure 19: The progressive pattern loaded in the Digital Signal Generator.

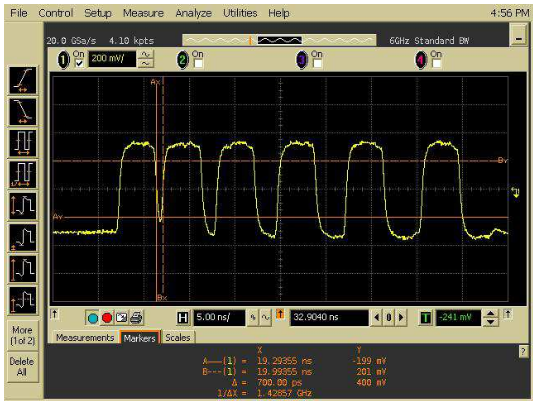


Figure 20: The progressive pattern at the Backplane output.

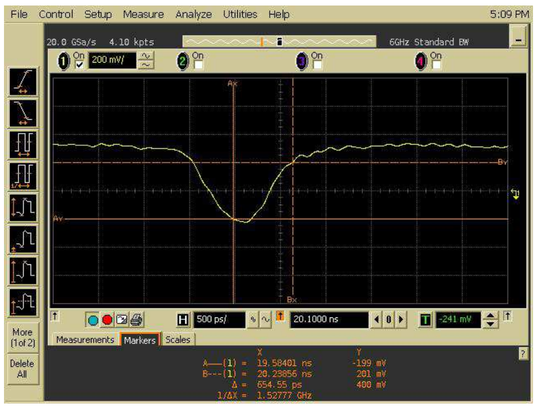


Figure 21: A detail of the previous image. The cursors represent the minimum level for the LVDS commutation.

with a low jitter (< 50 ps) and can manages a single pulse of ~ 850 ps.

[7] The minimum amplitude at differential probe is 400 mV, which coincides with a single signal of 200 mV.

4.5 Crosstalk

Crosstalk is an undesired effect, which appears on an electronic channel, when the electromagnetic interference, from another one, is not negligible. Crosstalk is usually caused by undesired capacitive, inductive, or conductive coupling from one part of a circuit to another. Therefore the main ingredients, which blow up this phenomenon, are high current, high frequency and geometry[8]. A couple of traces, which run close in parallel for a long space, has been selected for this test. With the help of specific PCB CAD tools, one of the worst case has been pinpointed (Fig.22). Those channels are number #111 with #151 (M9_30 & M9_31) and #230 with #285 (M3_1 & M3_5).

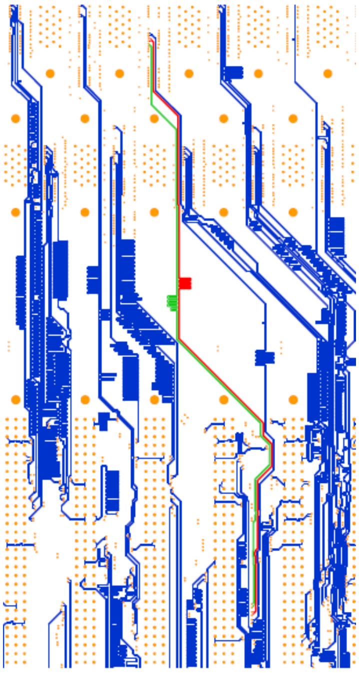


Figure 22: The neighbor channels #111 (green) & #151 (red) highlighted.

The aggressors are channels #111 & #230, which the progressive pattern has been injected in. The generated pulses have been terminated with a resistor of 100 Ω and have been saved on oscilloscope memory. The far-end crosstalk of victims is shown respectively on figures 23 & 24.

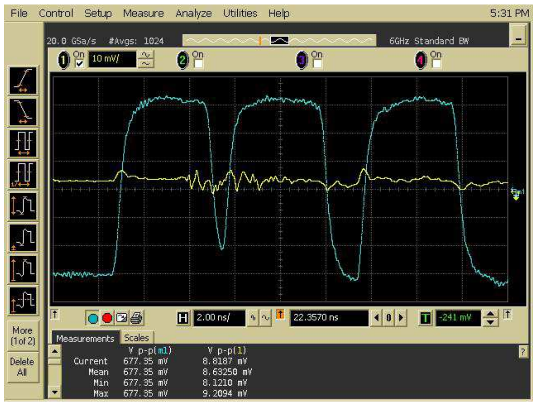


Figure 23: The image of the far-end crosstalk measured on victim M9_31 in average mode (256 samples).

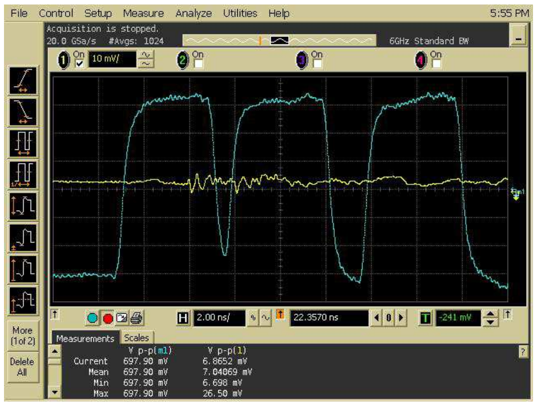


Figure 24: The image of the far-end crosstalk measured on victim M3_5 in average mode (256 samples).

The result is excellent because the V_{p-p} of victims is 8.8 mV (1.27 %) and 6.9 mV (1 %). Of coarse this is the crosstalk contribution due to the Backplane PCB. Another critical place could be the connectors, in particular *DIN 41612*, which are not shielded. Infact the crosstalk, measured on two close channels of connector M1, that are not contiguous inside PCB, is higher then before. The main contribution seems to be inductive and causes an effect of 12.2 mV_{p-p} (Fig.25), that corresponds to 1.84 %.

[8] The electromagnetic field between two wires changes in relation with distance and interposed mean.

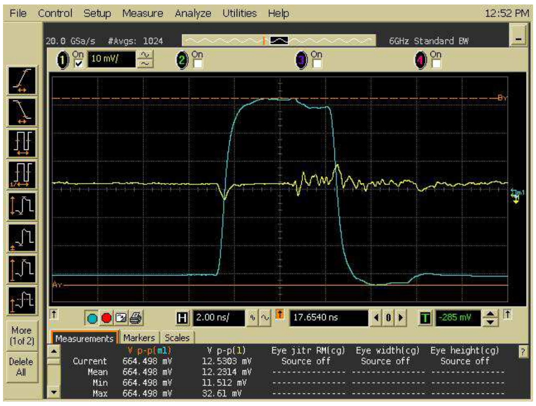


Figure 25: Crosstalk measured on connector *DIN 41612* between two close channels.

5 Conclusions

Backplane version 2.2 extensively respects the desired specifications, in terms of stability and high performances. The main features are an insignificant jitter (13 ps) and low skew (360 ps). This allows an easy synchronization of PMTs pulses, increasing the trigger efficiency. In addition, a bandwidth higher then 1 GHz and a well-done PCB layout ensure good signal integrity and the possibility to reduce the trigger gate, enhancing the noise rejection. Finally the probability of getting fake triggers is wiped out by the negligible crosstalk, which is less than 2.5 %.

Acknowledgments

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References

[1] F. Dazzi, *Realizzazione ed analisi del trigger di livello 1 del telescopio MAGIC*, Graduation Thesis in Physics, Padova 7 June 2001.

[2] D. Borla Tridon on behalf of the MAGIC Collaboration, *Performance of the Camera of the MAGIC II Telescope*, Proceedings of the 31^{st} ICRC, Lodz July 2009.

[3] Altera Corporation, *MAX 7000A programmable logic device family*, Altera Data Sheet ver. 2.03, September 1999.

[4] National Semiconductor, *An overview of LVDS technology*, AN-971, July 1998.