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Design and performance of an ultra low noise multichannel VCSEL pulser for MAGIC II receiver board testing

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Abstract

A compact four channel VCSEL pulse generator has been designed to test the MAGIC II receiver boards. This device imitates the signals supplied by the pixels of MAGIC II camera to the optical fiber links, by providing four channels with 1.3 ns pulses of 4 V. The design consists of a fast step recovery diode pulser, a 4-output resistive power divider, a 4-channel high power amplification stage and a board with VCSEL biasing circuitry. The modularity has been maximized while minimizing the lengths of the planar transmission lines. This enables an optimum performance in terms of pulse distortion, as well as robustness to interferences and crosstalk. The circuit operates with a single bias supply of 12 V. Pulse jitter measured with a 6 GHz oscilloscope is less then 10 ps. Pulse Repetition Frequency (PRF) jitter is less than 25 ns for a mean PRF value of 20 KHz.

Contents

1. How far can we go with standard components?

MAGIC II telescope will have a new generation of receiver boards with an improved bandwidth. The main purpose of the prototype presented here is to provide a portable unit able to test the proper operation of these receivers. To cover the full dynamic range of the VCSELs it is necessary to generate ns pulses with amplitudes in excess of 4 V. The specification for the optimum pulse width demanded by the receiver designers at IFAE was set to 1.3 ns. Other features such us low noise and low jitter as well as minimum ringing are also desirable.

These specifications are not easy to meet. The availability of commercial key components imposes some constraints to the figures of merit that can be achieved without relevant difficulties. Integrated SMD pulse generators are commercially available and can easily supply 5 V pulses to 50 Ω loads, but the corresponding widths hardly go below 5 ns. On the other hand, these generators are mainly intended to drive perfect resistive loads and are not well prepared to directly feed devices like LEDs or lasers, which exhibit noticeable impedance changes between their ON and OFF states. The issue of the generator sensitivity to load impedance changes is generally addressed by either inserting an attenuator or a buffer amplifier between generator and load.

RF monolithic (MMIC) amplifiers with bandwidths in excess of 1 GHz are also commercially available. However, mounting these devices on a printed circuit board for ns pulse amplification is not straightforward. The main difficulties to address are the resonances of the inductors, the parasitics of the grounding and the signal loss and distortion through the bias path. In practice it is hard to find MMIC amplifiers able to provide without distortion pulses of more than 4-5 V to 50 Ohm loads. These devices use to have fixed gains between 15 and 25 dB. Their biasing configuration makes difficult to tune the nominal gain by means of conventional feedback techniques. The gain tuning via bias control is also complicated due to the fact that these MMICs use to be designed to provide a stable gain with a very low sensitivity to bias voltage fluctuations.

The resonances of reactive components, especially inductors, play an important role in the bias networks of both pulse amplifiers and VCSELs when we want to work at frequencies above 300 MHz. High inductances (in excess of 100 nH) with high resonant frequencies and low quality factors are needed for biasing. High current operation is an extra demand for biasing amplifiers.

In the last years the market has seen significant improvements in the technology of SMD inductors. Today it is possible to find 10 μH inductors with resonant frequencies in excess of 100 MHz, but this is not enough to guarantee the lack of resonances in a usual bias network for a ns-range pulse amplifier with a bandwidth of 1 GHz. Therefore, in the design of the bias networks it is convenient to play with resistors in order to reduce the inductor quality factor and thus avoid distortion due to resonances.

2. The design concept

Figure 1 shows the schematics of the design. The number of different channels to be tested demanded the need for multiple generator outputs, which finally were set to four. This requirement immediately led us to decide on using amplification after power division.

The attenuators are necessary to minimize pulse distortion and ringing, which mostly occur at the output of the pulser and the input of the amplifiers. They also limit the amplitude levels at the

amplifier inputs to avoid their saturation. An even number of amplifying stages preserves the polarity of the Step Recovery Diode (SRD) pulser signals, since the best MMIC found for this application has a gain with a 180º phase shift.

The constitutive parts of the prototype (SRD pulser, power divider and amplifiers) were mounted in different boards and tested separately. The interconnections where made via SMA connectors and RG174 coaxial cables, and the RF paths were kept identical for all four channels. In order to accomplish this, it was necessary to design a power divider with a vertical input.

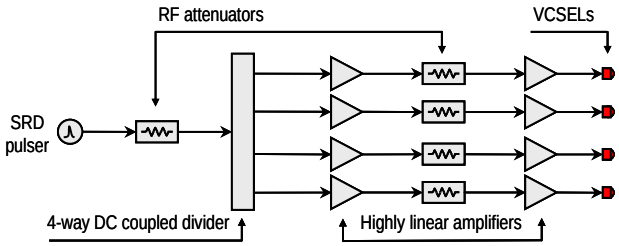


Figure 1. Design concept of the multichannel pulse generator.

The minimization of the cabling length was achieved by mounting the boards in a vertical arrangement, just like the pixel electronics of the MAGIC I and II cameras. With this arrangement the prototype is reasonably compact and free from long printed transmission lines, which could distort the pulses and make the prototype less robust against interferences. In addition, the four pulses at each channel are nominally identical and reach simultaneously the VCSELs, without any noticeable delay among them.

3. The Step Recovery Diode

Step Recovery Diodes (SRD) are P-I-N junction devices whose dynamic characteristics make them ideal to develop ultra-wideband RF devices such as frequency multipliers [1], sampling mixers [2], PLLs [3], and pulse generators [4][5][6][7][8]. An excellent study of these devices and applications to pulse generators can be found in the doctoral thesis of M. J. Chudobiak [9].

SRDs are fabricated with a quite narrow intrinsic region, and with very abrupt n and p doping distributions surrounding the intrinsic part. Figure 2 shows the electric field distribution in the i region of the SRD during a transient from a forward bias to a reverse one [10]. When the junction is forward biased, there is a strong accumulation of carriers at the i layer. Since this layer is very narrow, all the charge injected by a forward bias is stored close to the junctions. When the switching to reverse bias starts, the carriers start to deplete from the i layer, and an electric field starts to grow from the junctions [11], [12]. As a result, a reverse current is induced. When the i layer is about to be depleted from carriers (this is called the ‘punch through’ situation), an abrupt increase of the electric field occurs. This field strongly reduces the time needed to obtain a full depletion. In terms of currents, one can therefore identify three successive states:

1. The current initially corresponds to the one of a conventional forward-biased diode.
2. During the depletion a high reverse current exists until punch through occurs.

3. A fast transition to the normal negligible reverse saturation current takes place.

This behaviour of the current will clearly be seen in the simulation of the prototype (see Figure 4).

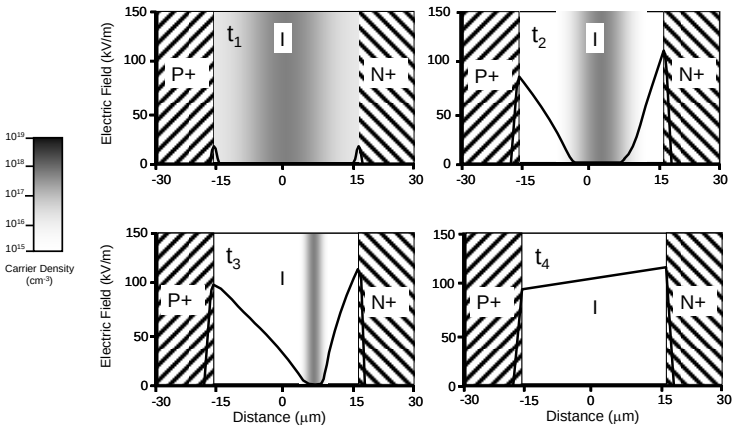


Figure 2. Electric field distribution in a SRD during a transit from a forward bias (t_1) to a reverse one (t_4) [10].

The simulation of the SRD dynamic characteristics has been the subject of intense research. The charge depletion after punch-through is so fast that its modeling poses severe numerical difficulties. However, we will show in the next section that a simplified model compatible with commercial CAD software provides a reasonable accuracy for ns range pulsers.

4. SRD pulser design

Figure 3 shows the schematic (a) and a photograph (b) of the constructed pulse generator. A low bandwidth pulser is applied to the series SRD. During the positive part of the pulse the diode is under forward bias, and the carriers are stored into the intrinsic region. The amount of stored charge, and thus the time-characteristics of the low and high state transitions of the diode, can be controlled by means of the time and amplitude of the forward bias.

The low bandwidth pulser (tens of nanoseconds) is used to feed the pulse-shortening circuit, consistent of a SRD, a shunt stub terminated in short-circuit and a Schottky diode. This generator is based on a Schmitt-Trigger inverter with asymmetric feedback. The charge and discharge of the input capacitor controls the input and output states of the inverter. When the capacitor is charged, the logic input is 1, and the output is 0. At this point, the capacitor discharges through the parallel of R1 and R2, as the diode is in ON mode. When the states are inverted, the capacitor charges through R2, so that the diode is in OFF mode. This way, both the repetition frequency and the pulse width of the low bandwidth pulser can be adjusted. A high value capacitor filters the DC component of the signal, so that its duty cycle determines the high and low voltages applied to the pulse shortening circuit. An accurate adjustment is of special relevance, so the charge and discharge times of the SRD and the voltage levels have a direct influence on the stored charge and so in the output pulse shape. The repetition frequency was set to 20 KHz and the voltage levels to 1 V and -2 V.

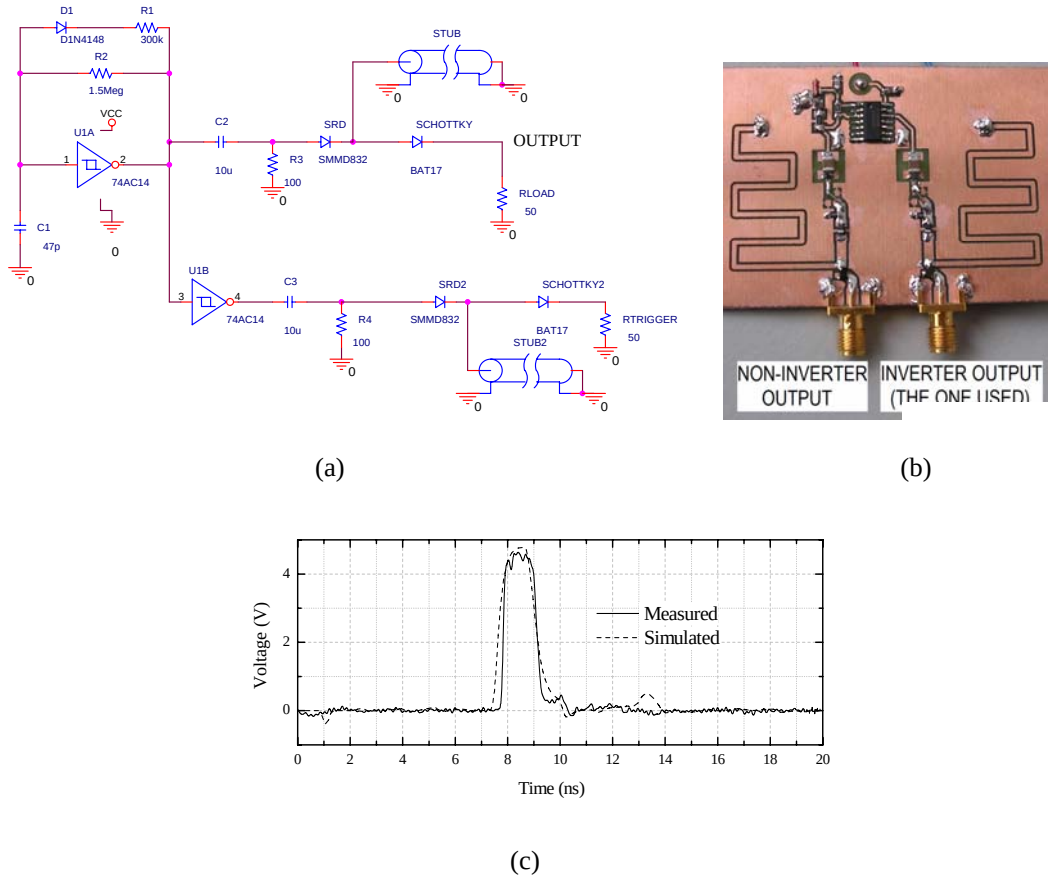


Figure 3. Schematic (a) and picture (b) of the Pulse Generator. (c) Simulation and measurement of the pulse.

The pulse-shortening stage works as follows (see figure 4). While the SRD (dashed line) is forward biased, the current corresponding to that voltage charges the intrinsic region of the junction. When reverse bias is applied the diode starts to discharge. A shunt, short-circuited stub (dotted line) sinks all the current provided by the SRD. But at high frequency the electrical length of the stub is not negligible, and there is a delay in the signal propagation towards the short circuit. This delay makes the current in the load to be the difference between the one provided by the diode and the one sunk in the stub. According to this, a negative and a positive pulse are produced in the flank of the current signal. The negative pulse is cancelled by means of a series Schottky diode (BAT17), and the positive one is driven to the load. This cancellation is made at the expense of reducing in ~200 mV the pulse amplitude. The simulation was made by removing the Schottky diode in order to visualize the negative pulse cancelled by this diode.

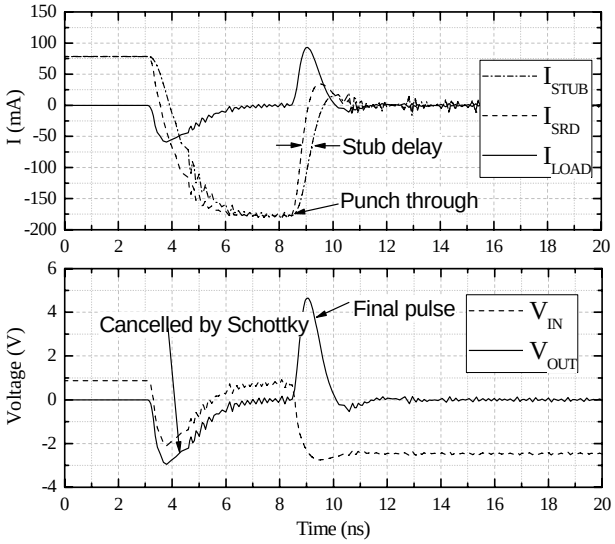


Figure 4. Pulse generator shaping. Top: Current in the diode ($\mathbf{I_{SRD}}$), stub ($\mathbf{I_{STUB}}$) and load ($\mathbf{I_{LOAD}}$). Bottom: Voltages at the input ($\mathbf{V_{IN}}$) and output ($\mathbf{V_{OUT}}$) of the SRD. The signals were simulated by removing the Schottky diode from the schematics of Figure 3(a).

The SRD diode used in this design was an Aeroflex-Metelics SMMD832 [13] with a transition time of 70 ps, carrier lifetime of 12 ns and a junction capacitance of 0.6 pF.

The pulse shape depends, apart from the SRD charge time, on the time delay of the stub and its impedance. An accurate modelling of the stub is critical to obtain a good simulation of the pulse width and amplitude. The stub designed for the pulser presented here was a coplanar line terminated in a via hole. This line transmits the pulse as a quasi-Transverse Electromagnetic Mode (quasi-TEM) with an associated effective permittivity and characteristic impedance that were both simulated with APLAC software. These values were then used to specify the equivalent coaxial transmission line parameters in the pulser simulation. It is not possible to achieve a good accuracy in the simulation if the planar stub is considered as a pure TEM coaxial line.

Figure 5 shows the dependence of the stub impedance and length on the pulse shape and amplitude. The final values of the coplanar line were 112 mm length, 1 mm width, and 0.5 mm gap between line and ground plane. The substrate was a FR4 laminate, with ε_r=4.5, substrate thickness of 1.57 mm and metallization thickness of 36 μm.

A good figure of merit of the pulse generator is the observed jitter, both in the repetition frequency and in the pulse width. These measurements were performed with an AGILENT infiniium 5855A digital store oscilloscope. Figure 6 (top) shows the histogram of the pulse width. The mean value is 1.324 ns and the jitter of the pulse width is a random Gaussian (no deterministic jitter has been observed) [14] with a variance of only 6.32 ps. This means less than 0.1‰ of the mean pulse width. The jitter of the repetition frequency is also a good figure of merit of the pulse generator. In Figure 6 (bottom) this histogram is shown, with a variance lower than 0.005‰ of the mean period.

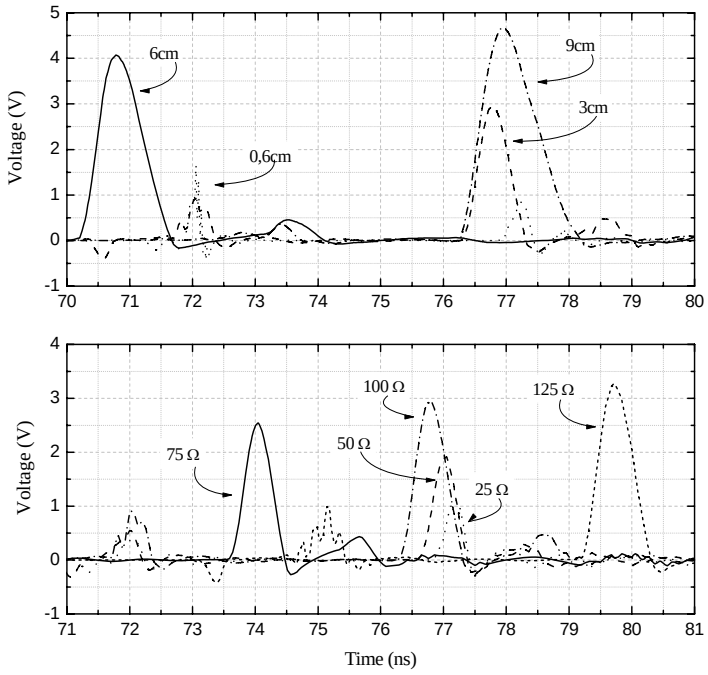


Figure 5. Effect of the stub length for a fixed impedance of 100 Ohm (top) and stub impedance (bottom) for a fixed length of 6 cm on the performance of the generator.

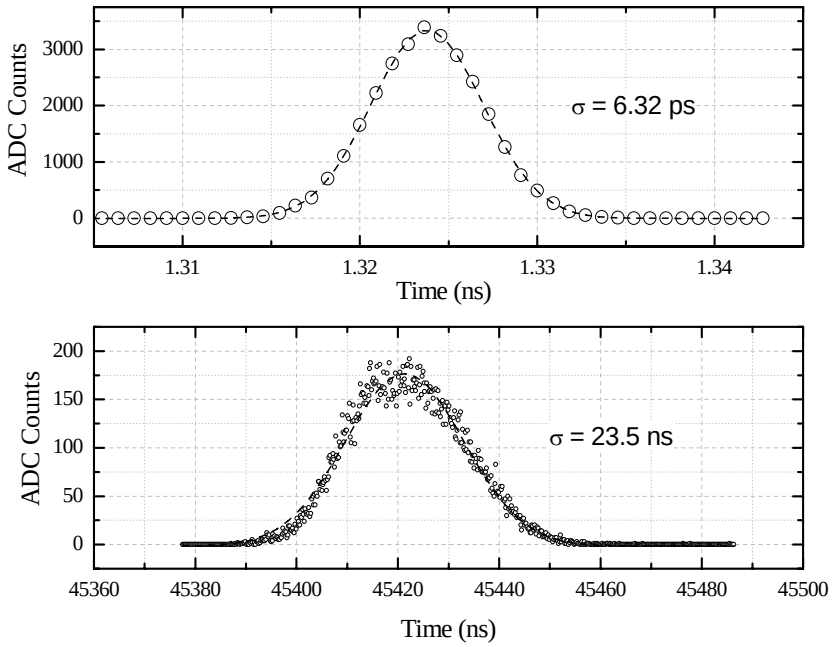


Figure 6. Top: pulse width histogram. Bottom: repetition frequency jitter.

5. Pulse division

One of the main issues to address in the design of broadband power dividers is the minimization of the junction reactive parasitics, which are sources of mismatches and therefore pulse ringing. This minimization can efficiently be accomplished by minimizing the final size and maximizing the symmetry of the design. Figure 7 shows the schematics of a DC coupled N-way resistive power divider of Z_0 impedance and $10\log_{10}(1/N)^2$ of insertion loss (a), and the final layout of the designed 4-way power divider (b).

The input resistance R_0 was mounted vertically inside a via hole opened in the board. This enables a compact design with all four outputs being perpendicular each other. The discrepancies in dB between the measured and theoretical (12.04 dB) insertion losses were less than 1%. Figure 7c shows the measured output waveforms, which are fully free from any ringing. In this measurement, a reference gaussian pulse of 4 ns width was applied to the input using a commercial 240 MHz bandwidth waveform generator (model Tektronix AFG3252).

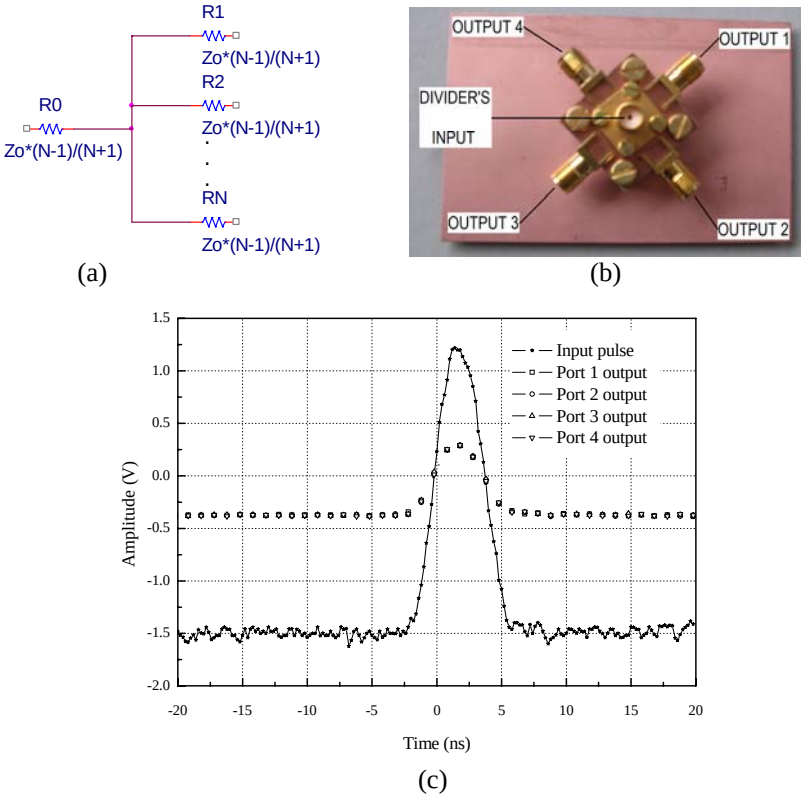


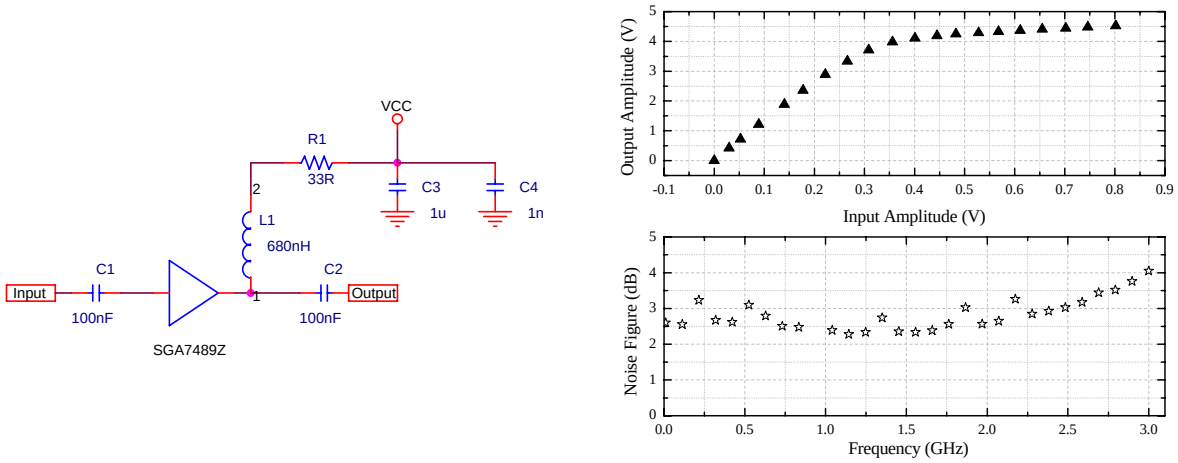
Figure 7. Schematics (a), final layout (b) and waveforms (c) of the power divider. The input pulse was generated with a commercial 50 Ohm waveform synthesizer.

6. Pulse amplification

In the selection of the amplifier three parameters were of special relevance: noise figure, dynamic range and bandwidth. Due to the short length of the pulse, an amplifier with bandwidth from DC to

at least 1 GHz was needed. The MMIC gain blocks basically consist of an inverting Darlington couple. This configuration yields to a 180º gain phase shift. Therefore, in order to have a positive output with a positive input two MMICs in cascade are needed. According to the Friis equation, the noise of the system is dominated by the input stage. The dynamic range is dominated by the output one. Several commercial amplifiers were studied in order to choose the one that fulfils the mentioned requirements.

The selected model, Sirenza 7489Z [15], is a low cost commercially available MMIC amplifier based on SiGe HBT technology, with 1 mm emitter Darlington configuration. This MMIC features 23 dB gain, 2.8 dB of noise figure and 1 dB compression point of 22.4 dBm at 850 MHz. The 3 dB bandwidth is 1 GHz. The MMIC was first mounted as a single stage amplifier on a FR4 substrate for test purposes. It was tested on the bias circuit detailed in Figure 8. Also shown are the measured values of the dynamic range in pulsed mode and the noise figure.



(a) (b)

Figure 8. (a) Schematic of the test circuit. (b) Upper graph: dynamic range of Sirenza 7489Z for negative, 4ns wide pulses. Lower graph: noise figure of the 1 stage amplifier board.

The dynamic range measurements were made with a sequence of 4 ns full width half maximum (FWHM) pulses of 1 MHz pulse repetition frequency. According to these measurements, the 22.4 dBm of 1 dB compression points yields to maximum saturation voltages of around 4.5 V. It is rather difficult to find in the market at the present moment RF MMIC amplifiers able to provide this range of linearity. The noise figure was measured with the noise measurement personality of the spectrum analyzer Agilent E4402B and the Agilent 346A calibrated noise source. Some spikes are shown in the noise figure curve which are not attributed to the amplifier but to external interferences. Despite them the noise figure of the mounted amplifier is fairly close to the one claimed by the MMIC manufacturer.

Figure 9 shows the measured and simulated frequency domain characteristics [16]. The simulation includes all the bias network and blocking cap parasitics, and it was made with APLAC software. The S parameter datasheet of the 7489Z is provided by the manufacturer. The stability factors show that the amplifier is unconditionally stable ($K>1$ and $|\Delta|<1$) in the whole range of frequencies. On the other hand, the low values of S_{11} and S_{22} show an excellent match to 50 Ohm. Finally, no significant resonances are observed in the gain factor (S_{21}).

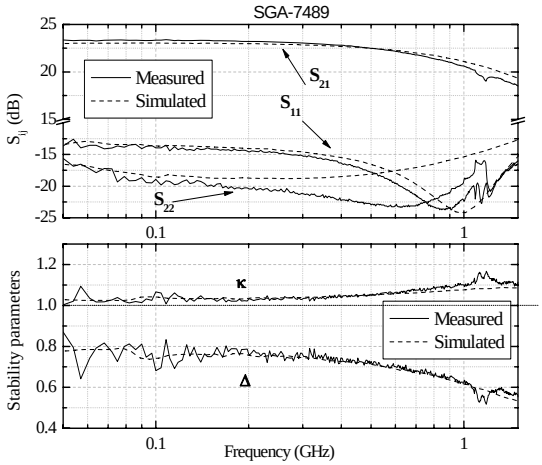
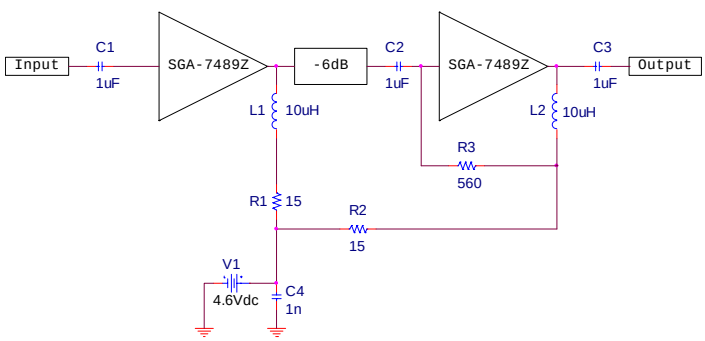


Figure 9. Top: S parameters of the tested amplifier. Bottom: Stability parameters. As it can be seen, the amplifier is unconditionally stable.

Once the single stage was tested we proceeded with a two stage design. The corresponding schematic is shown in Figure 10 (a). The second stage includes a feedback resistor to avoid saturation. Although this reduces the overall gain of the amplifier block, the present design already achieves the highest pulse voltages that can be obtained without saturating the two MMIC gain blocks.



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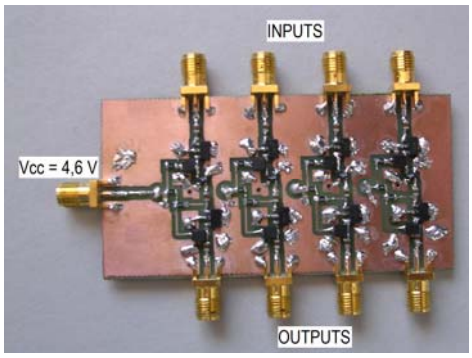

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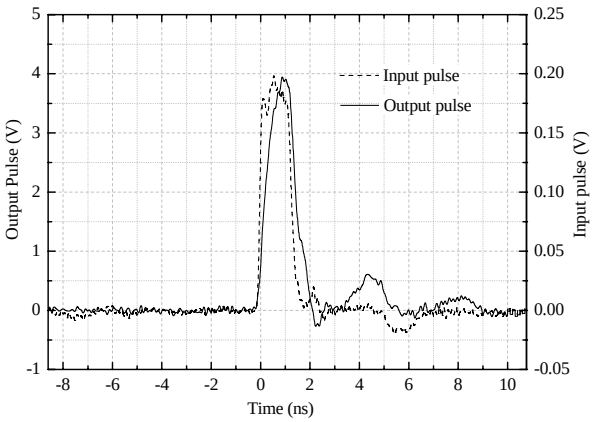


(c)

Figure 10. Shematic (a), final layout (b) and pulse shapes (c) of the two stage power amplifier used in each of the four output channels.

The attenuator between stages is an integrated 6 dB pad supplied by Minicircuits [17]. This pad prevents both saturation and distortion at the second stage, and avoids ringing between the different modules and stages. Measurements on the prototype show -20 dB of ringing level at the input (see dashed line of Figure 10, top). This ringing level is excellent in comparison with those found in recently published pulsers [6][7].

7. VCSEL biasing

Figure 11 shows the bias network designed to drive the VCSELs with a stabilized DC current. The topology is inspired in an improved version of the classical Howland constant current source [18], which is nicely described by Rafiei-Naeini and McCann in [19], and was proposed by MPI for the MAGIC II camera. In our design we include one operational amplifier (OPAMP) to drive only two VCSELs, which are modeled by 50 Ohm resistors. Therefore, we need two bias circuits. These approach has been followed in order to make use of low noise precision amplifiers, which are not able to drive the relatively large amount of current demanded by four lasers. The source labeled as 'Vcontrol' enables the tuning of the VCSEL current. The topology is designed to provide a stable VCSEL current I_{VCSEL} given by

$$I_{VCSEL} = \frac{V_{CONTROL}}{2R_{BIAS}}$$

The OPAMP is an OP27 low noise precision amplifier featuring a low 1/f noise corner with an input equivalent noise voltage of 3.5 nV/sqrt(Hz) at 10 Hz [20]. The low frequency noise injected to the VCSELs is thus minimized. Although this amplifier nominally works with bipolar biasing, a proper operation with an unipolar one was verified for DC. The possible distortion in the AC signal amplification is not relevant for this current source design.

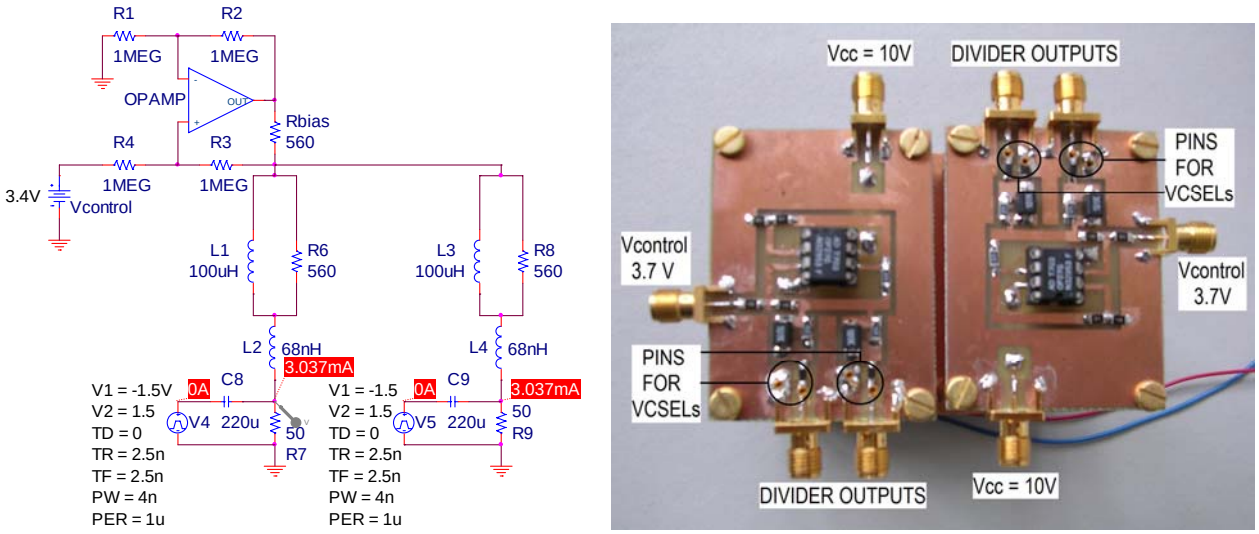


Figure 11. Bias circuit unit for each of the two pairs of VCSELs used in the board (a), and final layout arrangement (b).

In order to effectively block the pulse signal path to this bias circuit an inductive filtering implemented by L1, R6 and L2 is applied. One filter per channel is needed to prevent crosstalk between the DC paths of the lasers. Resistor R6 effectively reduces the resonant quality factor of L1. This enables the use of fairly high inductances without pulse distortion due to resonant effects. Other

filtering topologies were also tried (i.e. by using a capacitor between terminal 2 of L2 and ground) but the one shown here demonstrated the best behavior in terms of pulse shape integrity. Figure 12 shows an example of the signals measured at the four VCSEL signal ports. As it can be seen, the signals are free from ringing.

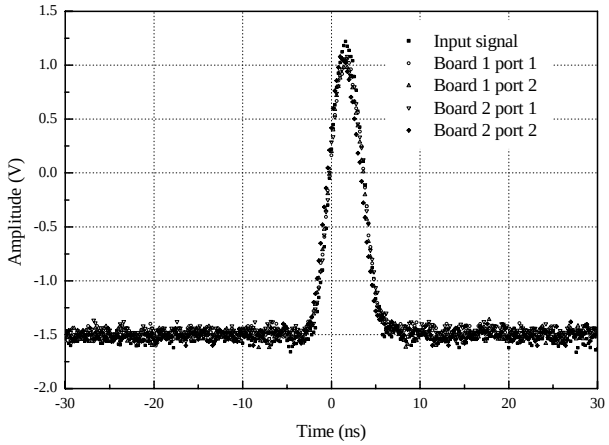


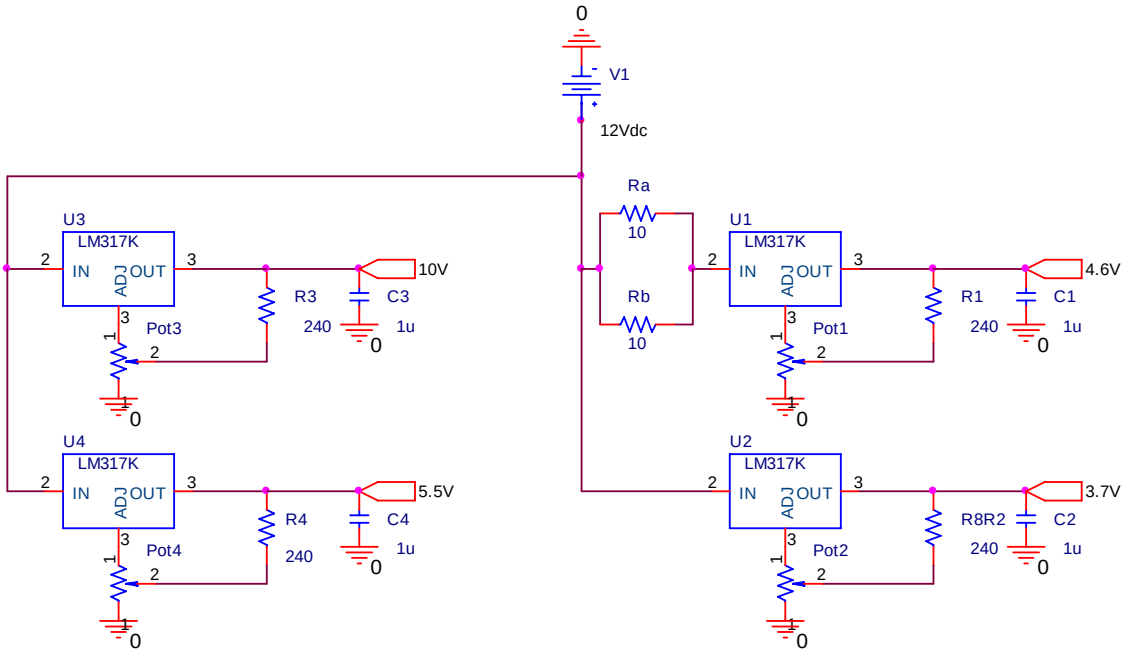
Figure 12. Pulse integrity at VCSEL pins contacts.

8. DC Regulation

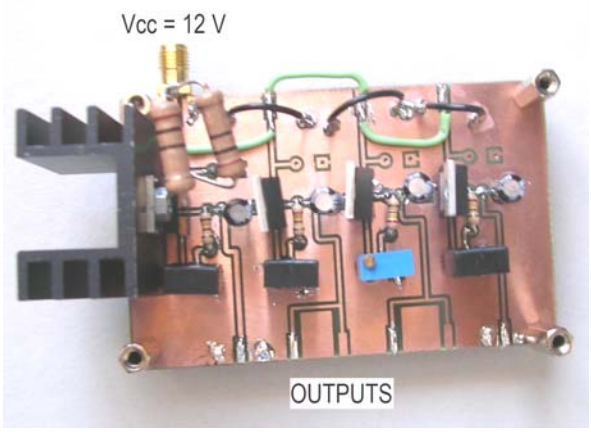
The DC regulation design strategy paid special attention to the noise performance. Many voltage regulators are important sources of noise, including voltage spikes from switching circuits and high 1/f noise form references which can exceed one microvolt per root-hertz. Three-terminal regulators use to generate hundreds of nanovolts per root-hertz of white noise. Switching regulators and DC to DC converters may have switching products of the order of millivolts which cover an unfairly wide range of frequencies.

Different procedures have been suggested to reduce the noise of DC regulation circuits. For instance, a large-value inductor combined with a capacitor or a clean-up regulator inserted between the noisy regulator and load. Other alternatives have been suggested to remove the undesired noise without directly handling the supply's high current [21].

Figure 13 shows the final regulation board. The multichannel pulser presented here features bias circuits for the pulse generator, amplification and VCSEL boards which have highly selective filters to avoid pulse distortion. On the other hand, the power consumption is not a critical issue for this application. Therefore the optimum choice for this case is a resistive three terminal regulation. The design proposed here makes use of four LM317 regulators to provide the four voltages needed: 10 V and 3.7 V for the VCSEL board, 4.6 V for the amplification board and finally 5.5 V for the pulse generator. All of them are fed by 12 V. The one feeding the amplification stage needs a special heat dissipation due to the high current consumption (600 mA). In addition, two power resistors in parallel are used in the channel for the amplifier bias to reduce the input voltage at its corresponding regulator and avoid strong heat dissipation at the regulator. When a source of poor stability is used, it could be convenient to add an extra input capacitor of around 0.1 μF.



(a)



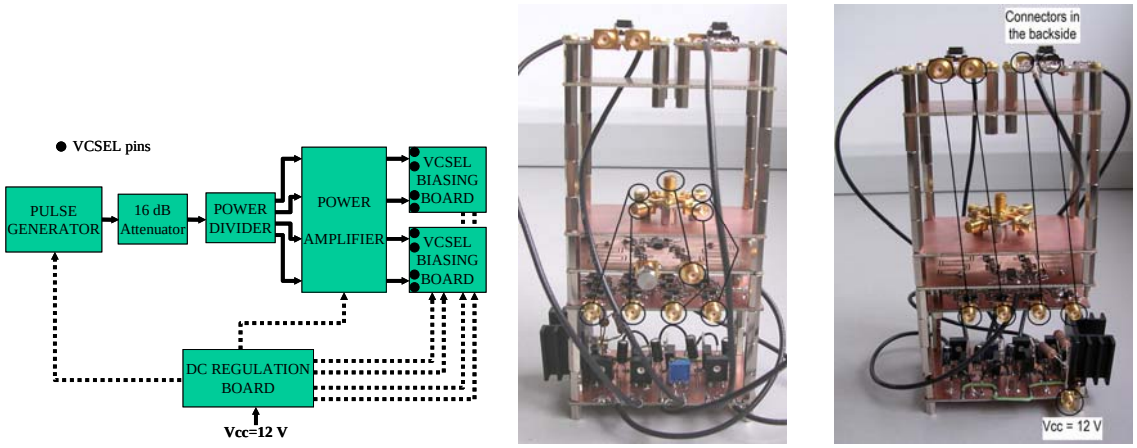
(b)

Figure 13. DC regulation board. (a) Schematic and (b) Picture. From left to right: one output of 4.6 V, 2 outputs of 3.7 V, 2 outputs of 10 V and one output of 5.5 V

9. Prototype structure and performance

Figure 14 shows a block diagram of the prototype including the DC paths, and two pictures showing the front and back sides, respectively. The black lines indicate the connections via coaxial SMA cabling. All the boards are FR4 laminates with 1.57 mm dielectric thickness. The 16 dB attenuator is a commercial SMA pad, which is not shown in the pictures. It avoids the saturation of the first amplifier and improves the versatility. In fact, with this pad one can make use of the 4 V pulser without the need for including extra attenuation. In addition, one can easily substitute the pad for a wide range variable attenuator to perform dynamic range tests. These units feature a relatively high residual attenuation, and therefore need high voltage pulsers. The boards shown in the pictures

are, from bottom to top, DC regulation, amplification, SRD pulser, power division, a laminate for mechanical stability and the VCSEL biasing.



(a) (b) (c)

Figure 14. Final prototype schematics (a), front (b) and backside (c) connections.

Figure 15 shows the output pulses injected into the VCSEL inputs. The peak amplitude of 4 V is achieved at the four channels without noticeable delays among them. The pulse width is 1.3 ns. The secondary peaks of 0.5 and 0.25 V were generated at the amplifier output as shown before, and are identical at all the channels. Therefore, they can be helpful to calibrate the saturation of the receivers by direct comparison with the detected amplitude of the main peak, without the need for using variable pulse amplitudes.

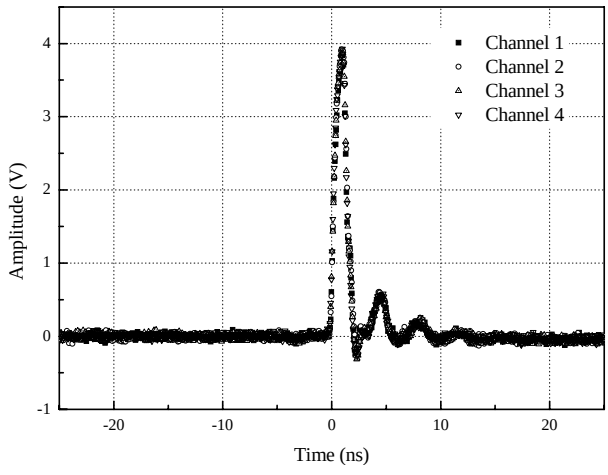


Figure 15. Amplification stage output signals

When operating the unit it is necessary to consider the following:

- Any port that is not being used must properly be terminated in 50 Ohm loads.
- The unit needs around two minutes for warming up.

- Care must be taken when working with the spendthrift and the power resistors of the DC regulation board. These devices work at high temperatures and could eventually harm the skin.
- DC regulation potentiometers must not be modified without a proper knowledge of how the DC currents will change. Improper handling of the potentiometers could produce permanent damage to the unit.

Acknowledgements

We want to dedicate this modest contribution to Florian. Florian Goebel was the first in suggesting us to work on portable ns pulsers for prototype testing. His dedication to MAGIC and his enthusiastic attitude to our work on high frequency electronics have always been a source of motivation and inspiration for the Madrid group. We will never forget him.

Pepe Illa has made valuable suggestions on how to optimize the main specifications of the prototype to better fit the design to the needs of the receiver board testing.

Eckart Lorenz has suggested us interesting ideas on the design of the prototype, especially concerning the power division.

David Fink has facilitated us all the details concerning the design of the MAGIC II VCSEL bias boards.

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List of components

Pulse Generator				
Component	Qty.	Package	Retailer / Manufacturer	Code
Inverter 74AC14SC	1	SOIC-14	Farnell	1014141
Resistor 100 Ohm	2	SMD 0805	Amidata	347-9780
Capacitor 47 pF	1	SMD 0805	Farnell	499160
Resistor 300 kOhm	1	SMD 1206	Farnell	1100256
Resistor 1.5 MOhm	1	SMD 0805	Farnell	9238018
Capacitor 10 uF	2	SMD 1210	Amidata	515-8485
Capacitor 1 uF	1	SMD 0805	Farnell	9227792
Fast Switching diode Fairchild 1N4148	1	DO-35	Farnell	9843680
Silicon Schottky Diode (NXP BAT17)	2	SOT-23	Farnell	1081187
Step Recovery Diode	2	SOD-323	MCE Metelics	SMMD840

Pulse Division				
Component	Qty.	Package	Retailer / Manufacturer	Code
Resistor 30 Ohm	5	SMD 0805	Farnell	6183151

Pulse Amplification				
Component	Qty.	Package	Retailer / Manufacturer	Code
Resistor 15 Ohm	8	SMD 0805	Amidata	347-9673
Resistor 560 Ohm	4	SMD 0805	Amidata	347-9881
Inductor 10 uH	8	SMD 1210	Amidata	548-2687
Capacitor 1 uF	12	SMD 0805	Farnell	9227792
Capacitor 1 nF	4	SMD 0805	Amidata	237-6977
SMD Attenuator DC-2500 MHz	4	MM168	Minicircuits	Lat-6+
MMIC Gain block	8	SOT-89	Sirenza Microdevices	SGA-7489Z

VCSEL Biasing				
Component	Qty.	Package	Retailer / Manufacturer	Code
Low Noise Precision OPAMP Analog Devices OP27EPZ	2	DIP-8	Amidata	522-8736
Resistor 1 MOhm	8	SMD 1206	Farnell	513090
Resistor 560 Ohm	6	SMD 1206	Farnell	9236805
Inductor 100 uH	4	SMD Type L	Amidata	367-4424
Inductor 68 nH	4	SMD 0805	Farnell	1198402

DC Regulation				
Component	Qty.	Package	Retailer / Manufacturer	Code
Regulator LM317TG	4	T0-220	Farnell	1130736
Trimmer 1kOhm	3	19 mm rect.	Farnell	1055409
Trimmer 5kOhm	1	19 mm rect.	Farnell	1055422
Resistor 240 Ohm	4	Axial	Farnell	6335366
Resistor 10 Ohm (2 watts)	2	Axial	Farnell	9338039
Capacitor 1 uF	4	Axial	Farnell	1161246