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Design, fabrication and characterization of a nanosecond pulse generator for the test of MAGIC optical links and DAQ system

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Abstract

A simple and cost-effective integrated synthesizer of fast pulses has been designed, assembled and tested for the integrity test of the optical links of the Telescope Camera. This synthesizer consists of integrated pulse generators based on Schmidt Trigger Inverters, 50 Ω matched passive attenuators and power dividers. It enables the generation of 2 ns pulses with 200 Hz repetition frequency, thus simulating the real Čerenkov light pulses. Three sets of outputs are provided, each set of different amplitude within the range 1mV – 1V allowing to test the linearity of the signal transmission chain.

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1. INTRODUCTION

A relevant task in the maintenance of the MAGIC Telescope camera is the test of the VCSELs, the optical link and the receiver boards. These tests can be simplified with the aid of a compact device able to generate the signals supplied by the PMT-preamp set to the VCSELs when the camera is illuminated by Čerenkov pulse radiation. Therefore, a pulse generator has been designed, fabricated and tested with this purpose in mind.-

The duration of the pulses to be generated is determined by the characteristics of the Čerenkov light and the PMT response. Taking into account these issues, a Full Width Half Height (FWHH) of 2 ns has been chosen as the key design specification. The amplitude of the pulses is set by the amount of photons incident on the PMT cathode and the gain of both the photomultiplier and the preamplifier in the base of the PMT. This is within the range of 1mV – 1V at the preamplifier output. Finally, the pulse repetition frequency should be close to the rate of events under real-world operating conditions, that is around 200 Hz.

In these tests, three identical outputs are needed. One is directly connected to the channel to be tested and the other two are used to generate a trigger via two additional channels. Therefore a 9-channel prototype has been developed with three sets of outputs, each one supplying three different voltage amplitudes: 2mV, 20mV and 700mV.

2. PULSE GENERATION

The Schmitt Trigger.

The theoretical basis of the developed pulse generator lays on the well known hysteresis behaviour of the Schmitt Trigger inverter.[1] As shown in Fig. 1, the asymmetry in the characteristics provide the generation of a square wave when the charge and discharge of a capacitor placed at the input is forced by means of a feedback resistance. The capacitor is initially discharged, so the input of the inverter is 0 and the output is 1. The current flows then through the resistance and begins to charge the capacitance, until the value V_{IH} is reached. At that moment, the output turns to 0, and the current changes its direction discharging the capacitor until V_{IL}, when the output changes to 1. The process is repeated once and again while the inverter is polarized, thus generating this way a symmetric square wave. The frequency can be controlled by means of the time constant RC. Figure 2 shows the capacitor curve (a), and the square wave generated (b).

The main difficulty of this step is to achieve a good time response, that is, to minimize the rise and fall time of the wave edges. Among the variety of Schmitt Triggers commercially available, one of the fastest belongs to the CMOS family (74AC14).[2] This technology fits well to the present purposes, as the power consumption is minimized (the quiescent supply current of the device is very small, up to a few μA), the edge transitions are symmetrical and have a duration of less than 2 ns.[2]

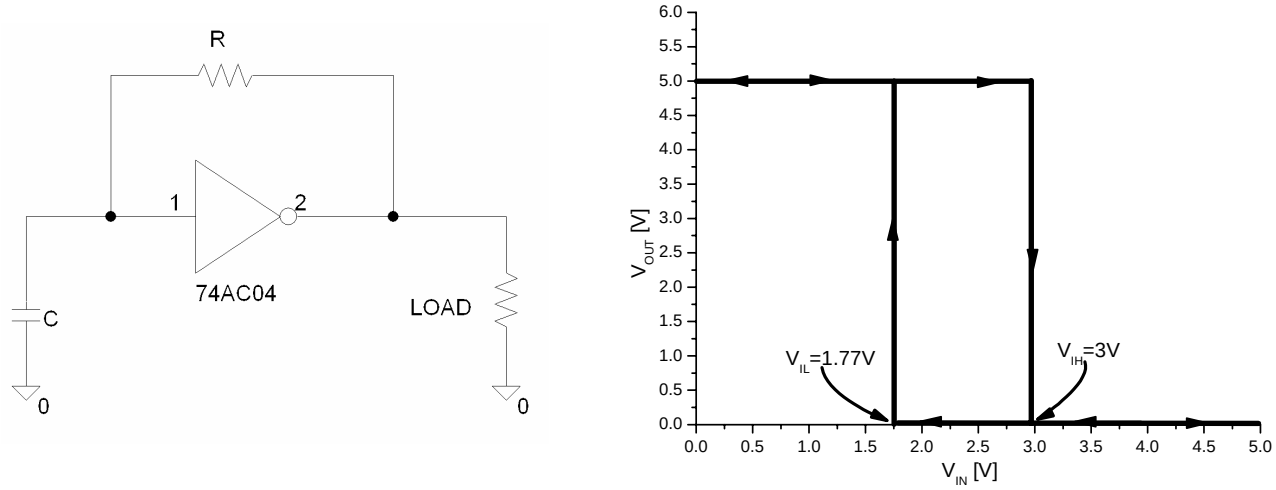


Figure 1. (a) Square wave generator. (b) Hysteresis curve of the 74AC14 HEX inverter.

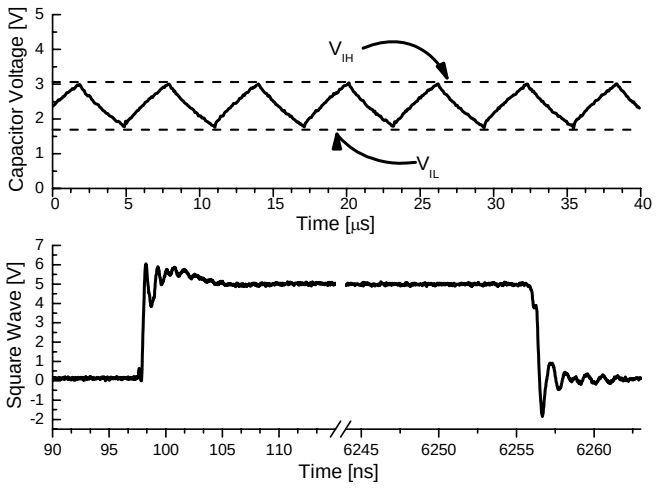


Figure 2: (a) Charge and discharge of the capacitor at the input of the inverter. (b) Rise and fall edges of the square wave.

Pulse shaping.

The straightforward step is to reduce the square wave into a narrow enough pulse. For this purpose, the usually annoying gate delays are used.

If the 'AND' function of a square wave and its inverted one is done, the result would be a logical zero. But as a certain delay exists in the propagation of the signal through each gate components, a 'glitch' will occur at the output of the AND gate (Fig. 3 (a)). This results in an output pulse, with an ideal amplitude of V_{CC} (logic gate bias), and a width that equals the delay of the inverter gate, typically 2-4 ns.[2]

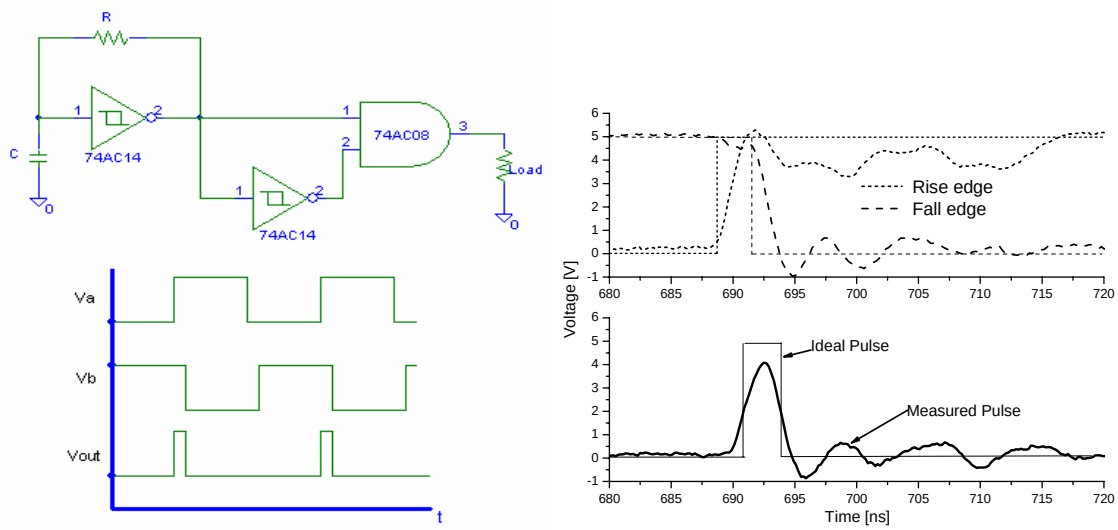


Figure 3. (a) Pulse generator based on the logical glitches (ideal response). (b) Actual generated pulse.

3. ATTENUATION AND MATCHING

Once a pulse of the desired width has been generated, it must be fitted to satisfy the amplitude requirements. This is achieved by means of passive attenuators,[3] designed to provide simultaneously the desired output level and the necessary impedance matching to the input of the VCSEL drive circuit.

The utilization of passive networks is a controversial issue. The main disadvantages are the obvious power consumption and the unavoidable introduction of noise in the signal. On the other hand, the advantages are an extremely easy design and implementation, not needing external bias and control as active elements do.

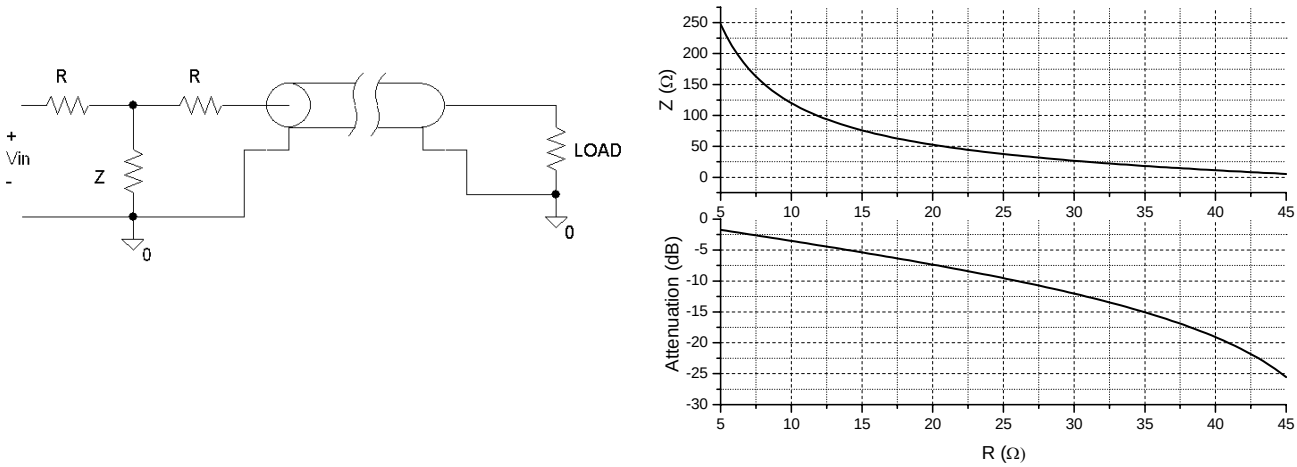


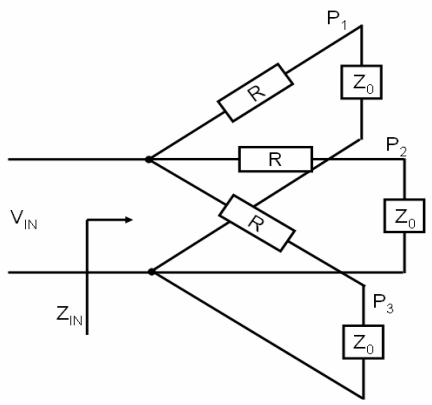
Figure 4. (a) Passive attenuator and transmission line schematic. (b) Graphs used for the design of the desired attenuator (50 Ω matched).

Taking into account that the transmission lines have a characteristic impedance of 50 Ω, the typical attenuation network can be implemented and synthesized as shown in Fig 4. The resistances are chosen for the attenuator to present 50 Ω impedance at both ports and to provide the desired attenuation as shown in Fig 4(b). For a given value of the attenuation, the lower graph sets the value of R, and the upper graph sets Z for that R, providing 50 Ω impedance at the input and the output.

4. POWER DIVIDERS

It is well known from Microwave Engineering that it is impossible to design a power divider that provides both perfect matching and no losses.[4] In the design of short pulse generators one of the most difficult issues is to achieve pulses free from ringing and distortion. This is usually accomplished by using dissipative networks, which decrease the amplitude and slightly degrade the noise figure. In this particular design this effect was partially compensated by tuning the attenuator losses.

As mentioned before, three outputs are needed for each value of the pulse amplitude, so the line coming from the attenuator must be splitted into three lines, each of them with an impedance that provides 50 Ω when viewed from the input port. The power delivered to each of the three loads (P_1, P_2 and P_3 in Fig. 5) is 1/9 of the input power and the losses in the resistances are 2/3 of the initially available signal power.

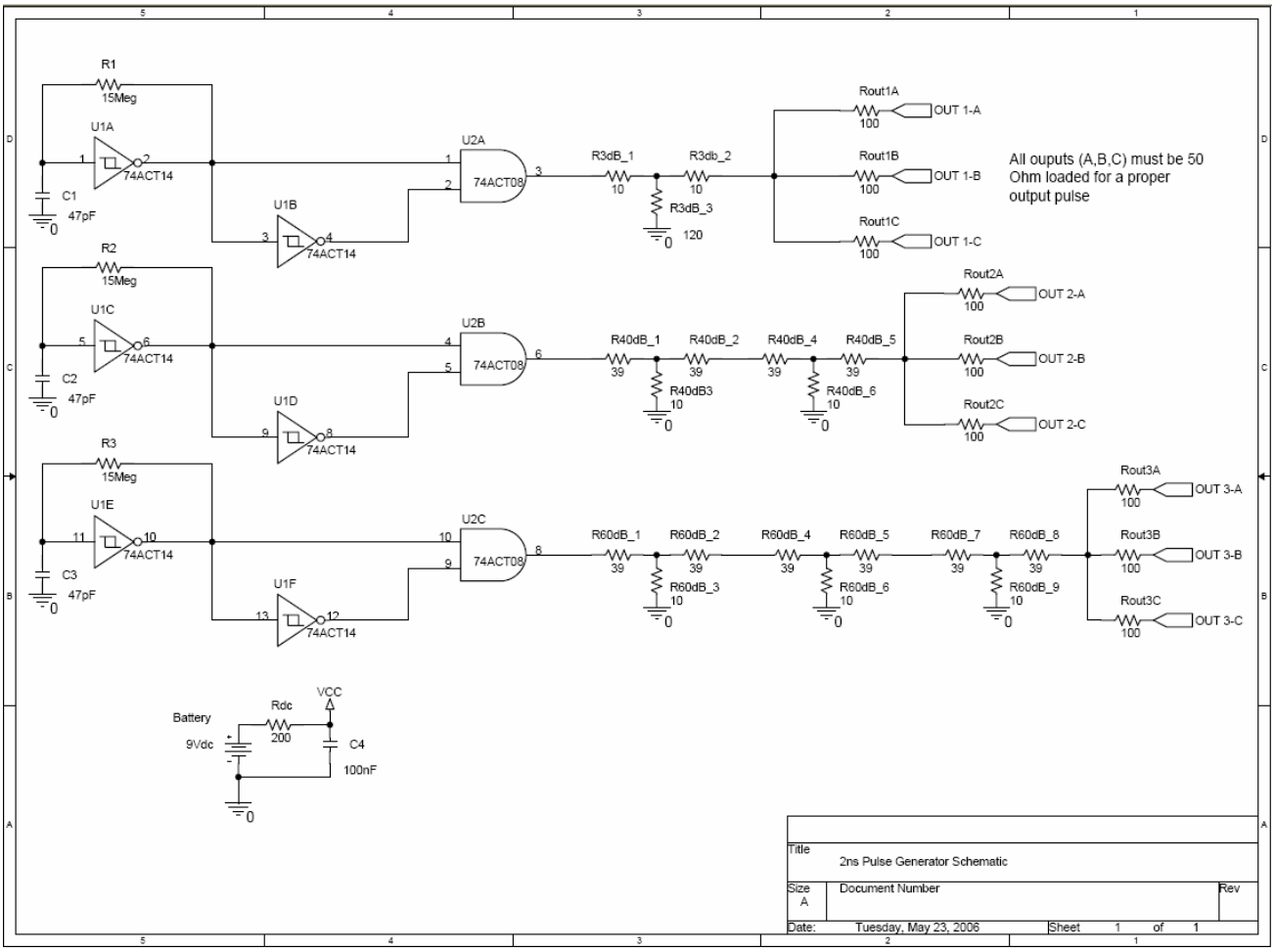


Parameter	Value	Parameter	Value
Z_0	50 Ω	V_1, V_2, V_3	$\frac{V_{IN}}{3}$
Z_{IN}	50 Ω	P_{IN}	$\frac{1}{2}\frac{V_{IN}^2}{Z_0}$
R	$2Z_0 = 100\Omega$	P_1, P_2, P_3	$\frac{1}{2}\frac{V_1^2}{Z_0} = \frac{1}{9}P_{IN}$

Figure 5. Values of the parameters for a 4 port, 50 Ω matched, passive power divider.

5. SCHEMATIC, LAYOUT AND PACKAGE

The schematic and layout of the pulse generator have been developed using ORCAD software (Capture CIS and Layout Plus, respectively) and are shown in Fig. 6.



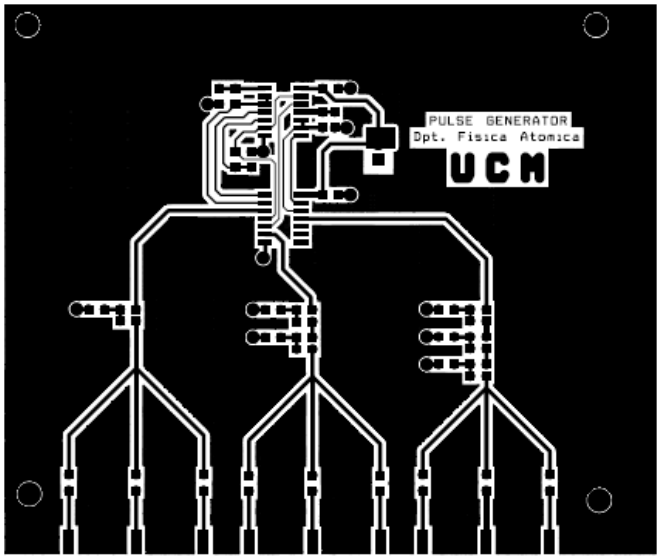


Figure 6. Pulse Generator (a) schematic and (b) layout.

Finally, the entire PCB and a 9V standard battery are enclosed in a plastic box, with front and back aluminium panels. In the front part, a switch controls the on/off position (confirmed by a LED), and a commuter selects between the normal operation and the battery test mode.

All the outputs are in the rear part of the box, divided into three sets of three identical outputs. The connectors used are 50 Ω coaxial female subminiature-A connectors (SMA).

Figure 7. Pulse Generator package.

6. PERFORMANCE

Once assembled, the data have been measured and acquired using a 6 GHz, 20GSa/s digital oscilloscope (AGILENT infiniium 5855A DS8).

Fig. 8 shows the actual generated pulses. For a given set of outputs, the three channels are perfectly synchronized. The noise is well below the sensitivity of the oscilloscope, as can be deduced from the fact that different measurements (in every channel, and even without the device connected to the input of the oscilloscope) show identical values of 390μV RMS.

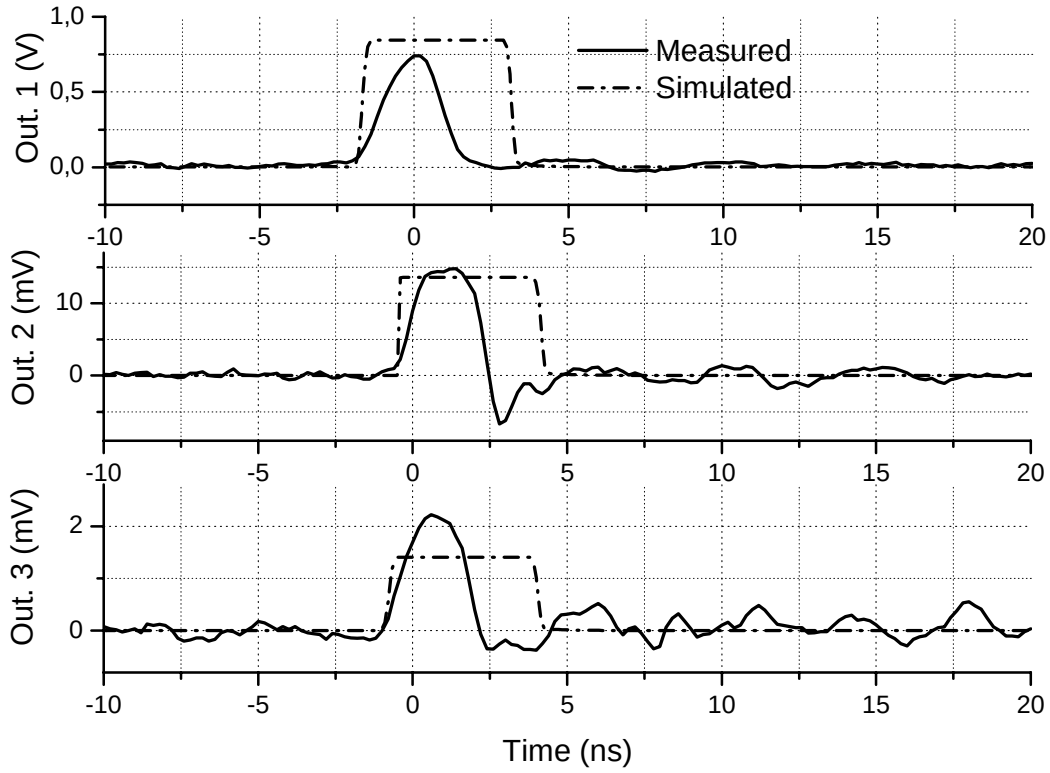


Figure 8. Measured and simulated pulses at the three different outputs.

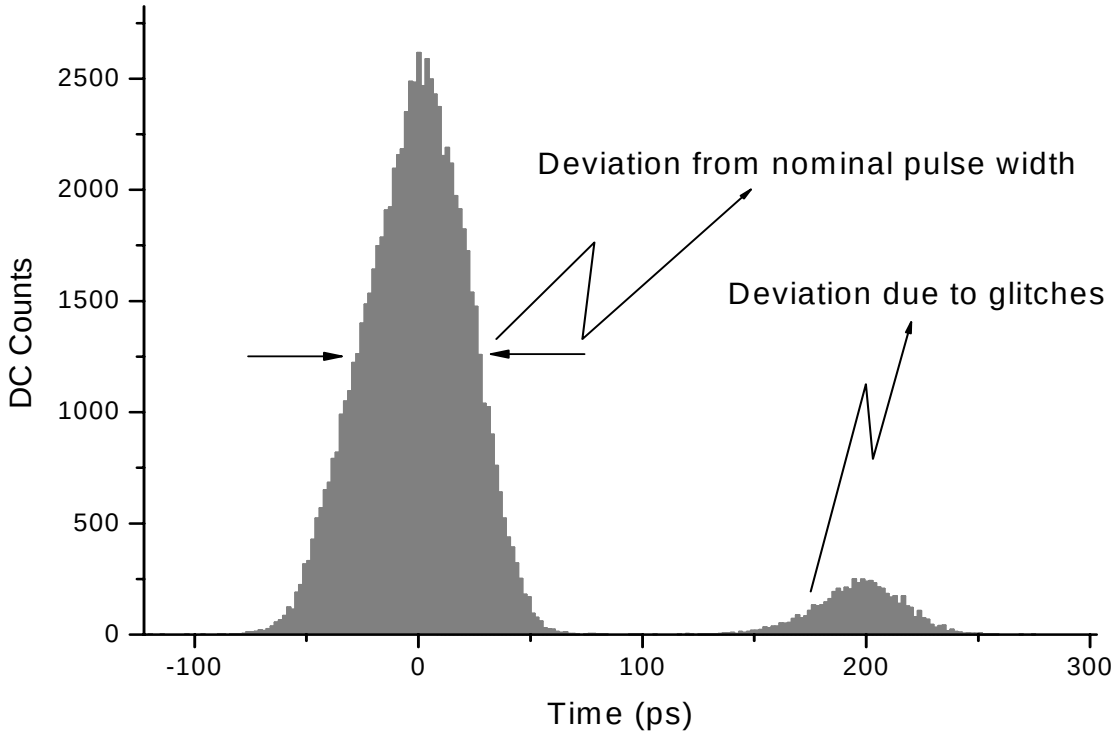


Figure 9. Jitter measurements. The standard deviation from the nominal pulse width is only 39 ps.

The stability of the pulse generator is very high. The pulse width jitter has been measured (Fig. 9), giving a standard deviation of 39 ps. Some systematic variation of the pulse width to a second discrete value (200 ps wider than the nominal value), due to glitches in the circuit performance, has been observed with probability lower than 8%.

REFERENCES

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