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Specifications of the digital DAQ modules and their digital inputs

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Abstract

Here we specify the purpose and design of the special DAQ FADC modules accepting digital inputs (the so-called dummy modules). We also attempt to identify all possible inputs which will enter these modules.

Contents

1 The general readout

The camera signals of the MAGIC telescope are digitized using fast Flash-ADCs (FADC). The FADC system and computer PCI readout have been described in detail elsewhere ([1, 2, 3, 4]. See the DAQ and general web pages in Munich for these documents). The multilayer trigger of the telescope is also fully documented in reference [5]. We will briefly describe here the trigger and FADC system of the MAGIC telescope, discuss how they are linked together and how time stamp and trigger features are latched with the events using special digital modules.

2 Trigger

The trigger in MAGIC is multilayer. The Cherenkov pulses in the photomultiplier anodes are transmitted from the camera at the telescope focal point to an electronics room over optical fibers. A discriminator at the receiver board provides a first level of trigger (what we may call level 0). The discriminator level is set remotely from the camera and calibration control.

The output of the discriminators is fed to the level 1 trigger (L1T). The L1T selects only time coincidences with a defined geometrical pattern (by default packages of 4 next neighbour pixels). The L1T rate may be as high as 100 MHz.

The L1T and the discriminator output are fed to the level 2 trigger (L2T). L2T applies a more sophisticated logic to produce a trigger rate that can be processed by the DAQ. The L2T can perform an online image analysis, for example it can provide a rough estimation of the γ-ray energy by looking at the number of pixels over the discriminator threshold and define different trigger types according to this energy estimate (low, mid and high energy). In addition the L2T accepts trigger signals coming from other sources: pedestal and calibrations. The L2T pre-scales all these triggers according to predefined ratios (e.g. allows 1 every 10000 low energy triggers, 1 every 100 mid energy triggers, all high energy triggers, all calibrations...). The trigger type is encoded in 8 bits that are transmitted to the FADC system (see below).

The prescaler generates what we will call low frequency (**LF**) trigger at rates $<$1 kHz. This LF L2T enters the FADC system at the central trigger and time unit (CTTU) and is distributed to all the FADC modules (see below for a full description of the FADC system). At arriving at the modules the digitized pulses are sent to a FIFO. The FIFO is asynchronously emptied by the DAQ computer. If the FIFO gets half-full, a BUSY signal is sent to the L2T in order to prevent additional triggers. This BUSY is reset when the FIFO is no longer half-full. Such a signal is essential because any deadtime in the DAQ system would affect the real trigger ratios in the L2T prescaler.

The DAQ can process a maximum sustained event rate of 1 kHz. However the L2T can generate up to $\sim$1 MHz trigger rates (This may be interesting at low energy thresholds or for very intense episodic sources: peak of GRB emission, AGN flares, pulsar main pulse...). In order to keep as much of this additional information as possible, the L2T will send a high frequency (**HF**) trigger over a second independent line. This HF trigger is prescaled too. It goes only to the special digital modules that are described in section 4 and independently latches the time stamp and the trigger pattern (in total 2 bytes) to the FIFOs. In this way a fixed number (??) of HF triggers are stored with each of the LF triggers. If less than this number of HF triggers arrives, the FIFO is padded with zeroes.

3 Analog modules

Each pixel line enters an electronic module that contains an 8-bit 300 MHz FADC, a 32 kB deep ring buffer and an FPGA, and has a corresponding 512 kB deep FIFO memory buffer on a base board. The base board holds 8 sockets for 8 FADC modules. A crate consists of 4 of these FADC base boards and an interface board. There will be a total of 19 crates, allowing a maximum of 608 modules. Each FADC module digitizes the analog pixel signal and writes the digitized data (time samples) to the ring buffer in real time (300 MHz per sample).

When the L2T arrives at the FADC modules, the FADC stops digitizing and the FPGA transfer a number of 1-byte time samples from the ring buffer into the FIFO. The *number of samples* (most probably 30) is set by the DAQ computer before proceeding to data taking.

For each 8-module FADC board we add two additional variables:

- The 42 MHz FADC clock tick at the time of the trigger (32 bits).
- A FADC event number: trigger processed by the FADC system (32 bits).

Both variables are stored together with the data for synchronization and test purposes.

A PC running Linux operating system reads all crates (including the special one) through a tree of interface boards and a PCI I/O card.

4 Digital modules

Apart from the digitized Cherenkov pulses, we would like to store additional data synchronously with each trigger. All the above-mentioned FADC modules accept analog signals as input, namely the Cherenkov electrical pulses in the camera photomultipliers. We will refer to them as **analog modules**. There will be also one 8-channel base board containing only special modules which directly accept "digital" information. These **digital modules** (or dummy modules, **DM**) work as "input registers".

4.1 Mechanical and electrical definition

Each of the DMs has 16 inputs which can be set to an LVDS 0/1 level. The 16 inputs make up two bytes that the FPGA saves to the module FIFO when a **HF trigger** arrives. This FIFO is filled up with new HF events until a new LF trigger arrives. The FIFO is then padded with zeroes until it contains a fixed *number of HF triggers*. In this way the DM can be read exactly like the standard analog modules.

The DMs have the same size of the analog modules and fit into the same sockets on the FADC board. The FADC board is standard.

The 16 inputs in the DM are implemented as a 40-pin socket for a 40-pin square flat connector like 3M 40-pin N3432-5002 (.100inch × .100 inch Latch/Ejector Header, 4 Wall, Straight and Right Angle, High Temp Option). A similar socket is shown in figure 1. Find also a description on the DAQ web page[6].

The electrical inputs are defined in the following table:

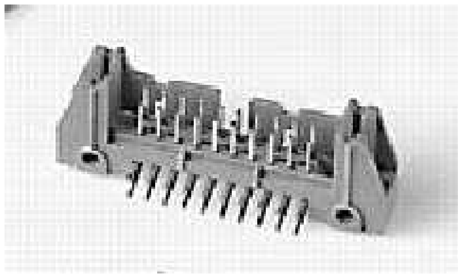

Figure 1: Detail of the input connector on the DM. Our connector has actually 40 pins.

GND	GND
GND	GND
D1	/D1
D2	/D2
...	...
D16	/D16
GND	GND
GND	GND

where the input signals are differential and Dn and /Dn is the signal corresponding to channel n. The signals are defined as LVDS digital levels.

The front of the metal box enclosing the board is left open. The flat cables going into the input sockets enter the board through this front opening.

4.2 Definition of the inputs

This subsection deals with the way bits are put into the various DMs. With this system up to 8 modules with 16 inputs each can be installed on a board. We shall refer to these modules as DM1-DM8. That corresponds to 128 inputs. For the moment we think on implementing only 5 DMS (DM1-DM5). That makes 80 digital inputs.

The purpose of the DM is to save digital event information that is synchronous with the LF and HF event. We have identified some of this information:

- A time stamp with < 1 μs accuracy.
- A trigger pattern that includes the kind of event, that is, Cherenkov shower, pedestal, light pulser calibration or diode calibration event, and any other information provided by the L2T.
- The whole calibration pattern encoded in 21 bits.

4.2.1 Time stamp

An atomic clock synchronized to GPS provides accurate time stamping down to 200 ns accuracy. This clock has two outputs:

- A flat cable with the 1 s - 400 day information. The lines in this flat cable are defined as follows:

contact	bit value	meaning
1 2 3 4	1 2 4 8	units sec
5 6 7	1 2 4	tens sec
8 9 10 11	1 2 4 8	units minutes
12 13 14	1 2 4	tens minutes
15 16 17 18	1 2 4 8	units hours
19 20	1 2	tens hours
21 22 23 24	1 2 4 8	units day
25 26 27 28	1 2 4 8	tens days
29 30	1 2	hundreds days
31 - 40	0 Volts (ground)	

We plan to record only the 1 s - 24 h information (20 bits). An adapter will be built from this cable to the connectors of DM1 and DM2. These inputs are defined as inputs 1-16 of the DM1 and inputs 1-4 of DM2. The order of the inputs is the same as in the output of the atomic clock.

- A coaxial cable with an LVDS digital pulse synchronized to the start of the second with 200 ns accuracy. This pulse resets a 5 MHz counter in the CCTU. The 5 MHz counter is based on a clock that is independent of the CCTU clock. An FPGA sends the contents of this counter (23 bits) to 23 outputs. This 23 outputs are connected to inputs 1-16 of DM3 and inputs 5-11 of DM2.

All in all the time information is encoded into 43 bits. This calls for 43 digital inputs, i.e., three almost full DMs.

4.2.2 Trigger pattern

The prescaler encodes the trigger type (energy estimate, calibration type...) in an 16 bit word: 8 bits for the prescaled pattern and 8 bits for the non-prescaled pattern. The actual pattern depends on the specific L2T table. A TDAS note is expected to document every new release of the trigger table.

Pedestal and calibration events are identified through electrical lines connecting the calibration system (CS) and the prescaler (through 12 reserved calibration input lines). Three output lines have been already defined in the CS:

- Light pulser line: set to 1 when the CS triggers the light pulsers and the L2T. It enters L2T line 3 (PULSE).
- Pedestal line: set to 1 when the CS triggers artificially the L2T to generate an event to study the FADC pedestal. It enters L2T line 1 (PED).
- Pin diode line: set to 1 when the CS allows the pin diode to trigger the L2T. The pin diode is triggered by a radioactive source at a fixed distance. It enters L2T line 4 (PIND).

The 16 lines coming from the L2T enter inputs 1-16 of DM4.

4.2.3 Calibration pattern

The previous schemes left inputs 12-16 of DM2 free. Additionally, 16 bits on DM5 are available for coding the calibration pattern:

DM 2:		
contact	1	0
12	Pure pulsar calibration: bits 1-16 on DM 5 give: pulse light pattern bits 13-16 on DM 2 not defined	No pure pulsar calibration
13	Pure continuous light calibration: bits 9-16 on DM 5 give: continuous light strength bits 12,14-16 on DM 2 not defined	No pure continuous light calibration
14	Continuous light calibration plus BLUE pulsed light bits 1-8 on DM 5 give: blue pulse light pattern bits 9-16 on DM 5 give: continuous light strength bits 12-13,15-16 not defined	No continuous light calibration plus BLUE pulsed light
15	not yet defined	not yet defined
16	not yet defined	not yet defined

DM 5:		
contact	meaning	addition explanation
1	5	GREEN PULSED
2	5	light strength
15	5	ONLY TOGETHER WITH:
16	5	BIT 12
3	5	BLUE PULSED
6	5	light strengh:
7	5	
8	5	every bit corresponds
9	5	to one LED slot
10	4	housing the number of
11	2	LEDs displayed in the
14	1	previous column
4	5	UV PULSED
5	5	light strength
12	5	ONLY TOGETHER WITH:
13	5	BIT 12
9	1	CONTINUOUS LIGHT
10	2	strength:
11	4	
12	8	ONLY TOGTETHER WITH:
13	16	BIT 13
14	32	or
15	64	BIT 14
16	128	

4.2.4 Others

Should we need any more inputs, additional modules DM6... DM8 may be built. Nothing in the architecture of the FADC system would prevent even further DMs in further 8-module boards.

References

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[5] “A two-level pattern-trigger for the MAGIC telescope”, D. Bastieri, M. Bettini, C. Bigongiari, D. Corti, R. Isocrate, M. Mariotti, L. Peruzzo, A. Saggion, P. Sartori et al. Nucl. Instrum. Meth. A 461 (2001), 521-523; and http://www.pi.infn.it/˜ paoletti/magic/trigl2/trigger-calibration.html

[6] http://hegra1.mppmu.mpg.de/MAGIC/private/science/daq/